Semiconductor Group Package Outlines

Reference Guide



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Semiconductor Group Package Outlines Reference Guide







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Preface

This document is a reference guide for packages used by the Texas Instruments Semiconductor Group in the manufacture of its integrated circuits.

Section 1 contains general information on the guide's content and description of package types available. It also includes information on packaging trends.

Sections 2 through 6 contain package outline drawings organized into five major sections: plastic/metal surface mount, plastic through-hole, ceramic surface mount, ceramic through-hole, and other packages. At the beginning of each section is a table of contents listing key information on each package.

The Appendix includes an alphanumeric cross-reference listing of packages by TI identification code. Also included is a glossary of packaging terms and other packaging handling and processing information.

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Purpose and Content

This document is a reference guide for packages used by the Texas Instruments Semiconductor Group in the manufacture of its integrated circuits. It includes outline drawings for 400+ packages currently available as well as other information to aid the customer in selecting the appropriate package for a specific application.

This guide is organized as follows:

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Alphnumeric	Index	1-10
Packaging I	rends	1-17
Plastic Surf	ace-Mount (Section 2)	Page
SOIC	Small-Outline IC	
HSOIC	Thermally Enhanced	2-12
SOP	Small-Outline Package	
HSOP	SOP With Heatsink	
SSOP	Shrink SOP	
HSSOP	Thermally Enhanced	2-38
TSOP	Thin SOP	2-39
TSSOP	Thin Shrink SOP	2-49
HTSSOP	Thermally Enhanced	
SOJ	J-Leaded SOP	
PLCC	Plastic Leaded Chip Carrier	
HPLCC	Thermally Enhanced	
DFP/TFP	Dual/Triple Flat Package	
QFP	Quad Flat Package	
BQFP	Bumpered QFP	
HQFP	Thermally Enhanced	
TQFP	Thin QFP	
HTQFP	Thermally Enhanced	2–140
Plastic Thro	ough-Hole (Section 3)	Page
PDIP	Plastic Dual-In-Line Package	
SDIP	Shrink Dual-In-Line Package	
TO/SOT	Cylindrical Package	
PFM	Plastic Flange Mount	
SIP	Single-In-Line Package	
HSIP	Thermally Enhanced	
ZIP	Zig-Zag Package	
OPTO	Light Sensor Package	
Caramia S:	rface-Mount (Section 4)	Doc:
JLCC	J-Leaded Chip Carrier	
LCCC	Leadless Ceramic Chip Carrier	
CFP	Unformed Ceramic Flat Package	
CEP	Formed CFP	



GENERAL INFORMATION

Ceramic	Chrough-Hole (Section 5)	Page
CERDIP		5–5
CDIP SB		5–11
CZIP	Ceramic Zig-Zag Package	
CPGA	Ceramic Pin Grid Array	5–20
Other Pa	ackages (Section 6)	Page
MQFP	Metal QFP	
BGA	Ball Grid Array	
MCM	Multi-Chip Module	
CSIP	Ceramic Single-in-Line Package	
Appendi	ix (Section 7)	Page
	Mount Using Preplated Leadframes	
	tatic Discharge (ESD)	
Moisture	Sensitivity of Plastic Surface Mount Packages	7_9
	ictures	
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Giossary	′	

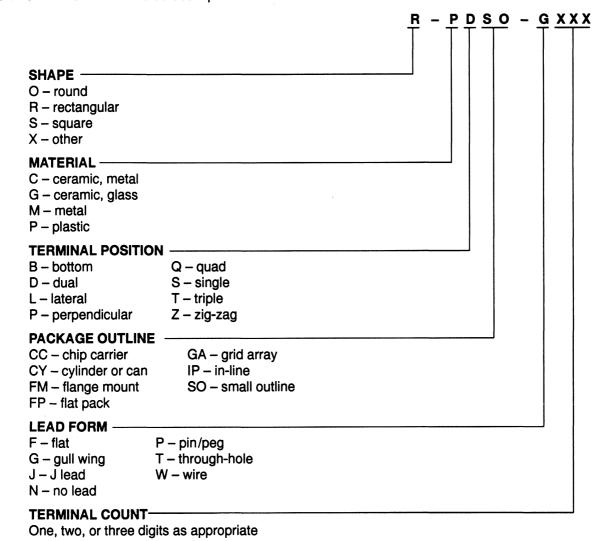
At the beginning of each package outline section is a table of contents that lists for each package the number of pins, descriptive remarks, TI package identification code, drawing and page references.

Drawings typically include the following dimensions: lead pitch (tip-to-tip); body width and length; shoulder-to-shoulder insertion; lead width, thickness, and angles; and package maximum height and stand-off clearance from seating plane to bottom of the package.

For packages designed in metric units, only millimeter dimensions are shown. For packages designed in English units, inch dimensions are shown first followed by millimeter dimensions in parentheses. A period is used as the English units decimal point, and a comma is used as the metric units decimal point.



Each package drawing contains a JEDEC Std 30 descriptor in the title line. This descriptor uses the following convention: shape, material, terminal position, package outline, lead form, and terminal count. The codes for each element in the JEDEC Std 30 descriptor are as follows:



SECTION 2 (Plastic Surface-Mount)

	DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
TSOP: TSSOP:	Small-Outline IC Small-Outline IC (Thermally Enhanced) Small-Outline Package (Japan) Small-Outline Package (Thermally Enhanced) Shrink Small-Outline Package Shrink Small-Outline Package (Thermally Enhanced) Thin Small-Outline Package Thin Shrink Small-Outline Package :Thin Shrink Small-Outline Package :Thin Shrink Small-Outline Package (Thermally Enhanced)	R-PDSO-G	
SOJ:	J-Leaded Small-Outline Package	R-PDSO-J	
PLCC: HPLCC:	Plastic Leaded Chip Carrier Plastic Leaded Chip Carrier (Thermally Enhanced)	R-PQCC-J or S-PQCC-J	Little Little
DFP: TFP:	Dual Flat Package Triple Flat Package	R-PDFP-G	L. L
QFP: TQFP: JM QFP: HQFP:	Quad Flat Package Thin Quad Flat Package JEDEC Metric Quad Flat Package Quad Flat Package With Heat Sink	R-PQFP-G or S-PQFP-G	ASSESSES AND
BQFP:	Bumpered Quad Flat Package	S-PQFP-G	The state of the s



SECTION 3 (Plastic Through-Hole)

	DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
PDIP: SDIP:	Plastic Dual-in-Line Package Shrink Dual-in-Line Package	R-PDIP-T	
TO/SO	T: Cylindrical Package	O-PBCY-W	
PFM:	Plastic Flange Mount	R-PSFM-T or R-PZFM-T	
SIP: HSIP:	Single-in-Line Package Single-in-Line Package (Thermally Enhanced)	R-PSIP-T	
ZIP:	Zig-Zag Package	R-PZIP-T	

SECTION 3 (Plastic Through-Hole) (Continued)

DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
OPTO: Light Sensor Package	R-PSIP-T or R-PDIP-T	

SECTION 4 (Ceramic Surface-Mount)

DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
JLCC: J-Leaded Chip Carrier	R-CDCC-J	त्री हो
	R-CQCC-J	
	R-GQCC-J	A CONTROL OF THE PARTY OF THE P
LCCC: Leadless Ceramic Chip Carr	ier R-CDCC-N or R-CQCC-N	

SECTION 4 (Ceramic Surface-Mount) (Continued)

	DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
CFP:	Unformed Ceramic Flat Package	R/S-CDFP-F R/S-GDFP-F R/S-CQFP-F R/S-GQFP-F	
CFP:	Formed Multilayer Ceramic Flat Package	R/S-CDFP-G R/S-CQFP-G R/S-GQFP-G	

SECTION 5 (Ceramic Through-Hole)

	DESCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE				
CDIP:	Glass-Sealed Ceramic Dip Package	R-GDIP-T	PRIPAPP				
CDIP SB	: Side-Braze Ceramic Dip Package	R-CDIP-T					
CZIP:	Ceramic Zig-Zag Package	R-CZIP-T					
CPGA:	Ceramic Pin Grid Array	S-CPGA-P					

SECTION 6 (Other Packages)

DES	SCRIPTION	JEDEC DESCRIPTOR	PACKAGE EXAMPLE
MQFP: Metal Qua	ad Flat Package	R-MQFP-G or S-MQFP-G	The state of the s
BGA: Ball Grid	Array	S-PBGA-N	
MCM: Multichip N	Module	Varies	
MEM MOD: Mem	ory Module	R-CDIP-N	



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DRAWING NUMBER	DSGN	PIN COUNT	PKG	PAGE NO.	DRAWING NUMBER	DSGN	PIN COUNT	PKG	PAGE NO.
4040192	AD	30	CSIP	6–26	4073275	DZC	50	SOP	2–64
4040196	BD	30	CSIP	6–27	4040136	FD	20/28/44/52/68/84	LCCC	4-12
4040197	BK	72	CSIP	6–29	4040137	FE	18/28/32	LCCC	4-11
4040226	BK	72	CSIP	6-30	4040221	FG	18	LCCC	4–9
4040047	D	8/14/16	SOIC	2–8	4040138	FH	20/28/44/52/68/84	LCCC	4-13
4040066	DA	28/30/32/38	TSSOP	2-50	4040139	FJ	44/68	JLCC	4–8
4040065	DB	14/16/20/24/28/30/38	SSOP	2-32	4040140	FK	20/28/44/52/68/84	LCCC	4-14
4040211	DBA	32	SOP	2-21	4040201	FM	18	PLCC	2-66
4040212	DBB	80	TSSOP	2-53	4040201	FM	22	PLCC	2-67
4040213	DBC	20(24)	HSOP	2-28	4040201	FM	32	PLCC	2-68
4040214	DBD	56	HSSOP	2–38	4040005	FN	20/28/44/52/68/84	PLCC	2-69
4040262	DBE	64	SSOP	2–35	4040142	FNC	24(28)	LCCC	4-18
4040263	DBF	80	SSOP	2–37	4040184	FNH	44	HPLCC	2-70
4040256	DBG	34	SOJ	2–63	4040143	FQ	20	LCCC	4-15
4040257	DBG	54	SOJ	2–65	4040159	FR	44	QFP	2-76
4073325	DBJ	44	SOP	2–23	4040160	FS	44	QFP	2-80
4073301	DBQ	20/24	SOIC	2-10	4040228-2		48	DFP	2-71
4040097	DD	32	TSOP	2-42	4040228-3		60	DFP	2-72
4040038	DF	30	SOP	2–20	4040229	FT	64	TFP	2-74
4040265-2		20(26)	TSOP	2–39	4040230-2		80	QFP	2-89
4040265-3		24(26)	TSOP	2–39 2–40	4040230-2		100	QFP	2-90
4040260-2		28	TSOP	2-41	4040141	FV	18	LCCC	4-10
4040260-2		32	TSOP	2-43	4040219	FZ	28/44/68	JLCC	4-7
4040200-3			TSOP	2–43 2–44					
		40(44)			4040114-2			CPGA	5-20
4040070-3		44	TSOP	2–45	4040114-3			CPGA	5–21
4040070-4		44(50)	TSOP	2-46	4040114-4			CPGA	5-22
4040070-5		64(70)	TSOP	2–48	4040114-5			CPGA	5–23
4040078	DGG	48/56	TSSOP	2–51	4040114-6			CPGA	5–24
4040068	DGH	64	SOP	2–24	4040114-7			CPGA	5-25
4073300	DGJ	50	TSOP	2–47	4040114-8			CPGA	5–26
4040092-2		20(26)	SOJ	2–55	4040114-9			CPGA	5–27
4040092-3		24(26)	SOJ	2–56	4040114-10			CPGA	5–28
4040092-4		28	SOJ	2–58	4040114-11			CPGA	5-29
4040048	DL	28/48/56	SSOP	2–31	4040114-12	GB-GA	19x19	CPGA	5-30
4073250	DLT	56	TSSOP	2–52	4040114-13	GB-GA	20x20	CPGA	5-31
4040046	DNA	8	SOIC	2-7	4040035	GF	325	CPGA	5-32
4040037	DP	48	SSOP	2-33	4040186	GFM	225	BGA	6–17
4040250	DQ	60	SSOP	2-34	4040185	GFN	256	BGA	6-18
4040091	DSA	20	HSOP	2-26	4073200	GFT	352	BGA	6–19
4040215-2		20	HSOP	2-27	4073201	GFW	388	BGA	6-20
4040215-3		24	HSOP	2–30	4073163	HAF	208	CFP	4-57
4040264	DT	36	SOP	2-22	4040163	HB	68	CFP	4–31
4040098	DT	70	SSOP	2–36	4073161	HBG	120	CFP	4–37
4040076	DV	28	SOIC	2-11	4081527	HBM	256	CFP	4–37 4–65
4040070	DW	16/20/24/28	SOIC	2-11	40401527	LIDIM	200	CED	4-00



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4040061

4040259

4040096

4040295

4073226

4073227

4073228

4040060

4040094-2 DZ

4040094-3 DZ

4040094-4 DZ

4040094-5 DZ

4040094-6 DZ

DW

DWA

DWB

DWH

DWM

DWP

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4040232

4040118

4040231-2 HFG

4040231-3 HFG

4040231-4 HFG

4040231-5 HFG

4040231-6 HFG

HD

HDI

HE

HFA

HFH

HFH

HFH

HFH

HGA

80

408

100

256

84

100

132

172

196

256

288

320

352

128

CFP

MCM

CFP

CFP

CFP

CFP

CFP

CFP

CFP

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CFP

CFP

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4073158	HH	96	CFP	4-50		4040209	ΚV	5	TO/SOT	3–29
4040144-2		20	JLCC	4–5		4040233	KV	7	TO/SOT	3–31
4040144-3	HJ	28	JLCC	4–6	1	4040003	KVA	15	PFM	3–52
4040174	HK	20	CFP	4–24	1	4040204	KVS	15	PFM	3–51
4040119	HKA	28	CFP	4–27		4040198	KW	8	PFM	3-49
4040120	HKB	28	CFP	4–28		4040199	KWV	8	PFM	3–48
4073160	HKC	64	CFP	4–30		4040235	LL LP	3	TO/SOT TO/SOT	3–25
4040145 4040146-2	HL HM	20 20	LCCC LCCC	4–16 4–17		4040248 4040001	LP	2 3	TO/SOT	3–21 3–22
4040146-2		28	LCCC	4–17 4–19	Ī	4073350	LPB	3	TO/SOT	3–23
4040117	HP	144/160	CFP	4–53	l	4040249	LPF	3	TO/SOT	3–24
4040121	HPA	208	CFP	4–58		4040020	MAA	100/132/196	MQFP	6–7
4040113	HPC	240	CFP	4–60		4040021	MAB	100/132/196	MQFP	6–8
4040071	HS	100	CFP	4–36	l	4040044	MBM	100	MQFP	6–5
4040169-2		84	CFP	4–34		4040019	MBN	100	MQFP	6–6
	НТ	132	CFP	4-39		4040043	MCM	120	MQFP	6–9
	HT	172	CFP	4-41	l	4040009	MCN	120	MQFP	6-10
4040169-5	HT	196	CFP	4-43		4040042	MDM	144/160	MQFP	6-11
4040170	HU	196	CFP	4-56		4040010	MDN	144/160	MQFP	6-12
4040072	HV	68	CFP	4-32	ľ	4040006	MEO	208	MQFP	6-13
4040112	HY	160	CFP	4-54	l	4040008	MEP	208	MQFP	6-14
4040073	HZ	176	CFP	4–55	1	4040013	MFO	240	MQFP	6–15
4040083	J	14/16/18/20/22	CERDIP	5–6		4040007	MFP	240	MQFP	6–16
4040084	J	24/28/32/40	CDIP	5–14		4040080	N	64	PDIP	3–14
4040223-2	JC	40	CDIP	5–16		4040049	N	14/16/20	PDIP	3–6
4040223-3	JC	64	CDIP	5–17		4040051	N	22/24	PDIP	3–10
4040086	JD	16/18/20/24	CDIP	5–11		4040053	N	24/32/40/48/52	PDIP	3–12
4040088	JD	18/20/22	CDIP	5–13		4040054	NE	16/20	PDIP	3–7
4040087	JD	24/28/40/48/52	CDIP	5–15		4040033	NF	28	SDIP	3–17
4040089	JD	64	CDIP	5–18		4040057	NF	30	SDIP	3–18
4040090	JDB	18/20	CDIP	5–12		4040034	NJ	40/54	SDIP	3–19
4040107 4040108	JG JK	8 24	CERDIP	5–5		4040153	NK	22 64	PDIP	3–11
4040108	JL	20	CERDIP CERDIP	5–9 5–7		4040056 4040032	NM NN	22	SDIP SDIP	3–20 3–15
4040109	JT	24/28	CERDIP	5–7 5–8		4040032	NN	24	SDIP	3–15 3–16
4040111	JW	24	CERDIP	5–0 5–10		4040075	NP	28	PDIP	3–10 3–9
4040207	KC	3	TO/SOT	3–10		4040062	NS	14/16/20/24	SOP	2–17
4040208	KC	5	TO/SOT	3–28		4040050	NT	24/28	PDIP	3–8
4040251	KC	7	TO/SOT	3–30		4040294	NU	8	OPTO	3–65
4040290	KCB	3	TO/SOT	3–32		4040079	NW	24/28/40/48	PDIP	3–13
4040205	KFA	9	PFM	3-41		4040296	NWM	28	MCM	6-22
4040291	KGC	9	PFM	3–42		4040082	Р	8	PDIP	3–5
4040059	KL	18	HSOP	2-25		4040036	PA	104	MCM	6-24
4040203	KN	15	PFM	3-45		4040275	PAB	136	QFP	2-100
4040252	KPA	3	TO/SOT	3–26		4040274	PAC	128	HQFP	2-104
4073383	KTA	9	PFM	3-43		4040276	PAD	44	QFP	2-75
4073384	KTB	9	PFM	3–44		4040271	PAF	80	QFP	2-83
4073385	KTC	15	PFM	3–46		4040282	PAG	64	TQFP	2-125
4073386	KTD	15	PFM	3–47		4040281	PAH	52	TQFP	2-124
4073375	KTE	3	PFM	3–33		4040278	PAJ	64	HTQFP	2–140
4073376	KTF	3	PFM	3–34		4040270	PAK	64	QFP	2–81
4073377	KTG	5	PFM	3–35		4040272	PAL	100	QFP	2–85
4073378	KTH	5	PFM	3–36		4040014	PB	120	QFP	2-93
4073379	KTJ	5	PFM	3–37		4040127	PBE	120	HQFP	2–108
4073380	KTK	7	PFM	3–38		4040155	PBG	52	TQFP	2–126
4073381	KTL	7	PFM	3–39		4040279-2	PBK	120	TQFP	2–133
4073382 4040210	KTM KV	7 15	PFM PFM	3–40 3–50		4040279-3 4040154	PBK	128	TQFP	2-134
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4040015	PC	144/160	QFP	2-95	4040045	PQ	100/132	BQFP	2-103
4040288	PCA	100	HTQFP	2-142	4040027	PR	128	QFP	2-88
4040202	PCB	100	HTQFP	2-143	4040063	PS	8	SOP	2-16
4040238	PCD	144/160	HQFP	2-109	4040052	PT	48	TQFP	2-122
4040237	PCE	144/160	HQFP	2-110	4040216	PTA	64	TQFP	2-123
4040024	PCM	144/160	QFP	2-96	4040157	PU	32	TQFP	2-120
4040103	PCY	144/160	HQFP	2-111	4040064	PW	8/14/16/20/24/28	TSSOP	2-49
4040239	PCZ	144/160	HQFP	2-112	4073225	PWP	20	HTSSOP	2-54
4040039	PD	54	MCM	6-23	4040149	PΖ	100	TQFP	2-132
4040148	PDB	304	HQFP	2-118	4073179	PZT	100	TQFP	2-131
4073180	PDN	304	QFP	2-102	4040151	RC	52	QFP	2-77
4073181	PDR	76	DFP	2-73	4040190-2	SC	4	SIP	3-56
4040099	PE	44	QFP	2-78	4040190-3	SC	10	SIP	3-60
4040067	PF	64°	QFP	2-79	4040206	SD	20/24/28	ZIP	3-63
4073175	PFA	100	TQFP	2-130	4040255	SE	4	SIP	3-57
4073176	PFB	48	TQFP	2-138	4040292	SK	7	SIP	3-59
4073177	PFC	80	TQFP	2-128	4040253-2	SL	2	SIP	3-53
4040101	PG	64	QFP	2-82	4040253-3	SL	3	SIP	3-54
4040026	PGC	240	QFP	2-101	4040254	SLL	3	SIP	3-55
4040156	PGD	144	TQFP	2-135	4040189	SM	14	SIP	3-61
4040147	PGE	144	TQFP	2-136	4040188	SP	4	SIP	3-58
4040134	PGF	176	TQFP	2-139	4040293	SR	3	OPTO	3-64
4040222	PGG	144	QFP	2-92	4040002	SV	20	CZIP	5-19
4073173	PGH	256	QFP	2-99	4040179	U	10	CFP	4-20
4040277	PGJ	128	QFP	2-91	4040193	U	30	CSIP	6-28
4073172	PGK	256	HQFP	2-115	4040172	VF	32	TQFP	2-121
4040247	PGV	240	HQFP	2-116	4040173	VG	100	HTQFP	2-141
4040245	PGY	240	HQFP	2-117	4040177	VH	100	HQFP	2-107
4040011	PH	80	QFP	2-84	4040180	W	14	CFP	4-21
4040012	ΡJ	100	QFP	2-86	4040180	W	16	CFP	4-23
4040123	PJE	100	HQFP	2-105	4040180	W	20	CFP	4-25
4040093	PJF	100	HQFP	2-119	4040180	W	24	CFP	4-26
4073174	PJG	100	HQFP	2-106	4040178	WA	14	CFP	4-22
4040022	PJM	100	QFP	2-87	4040176	WD	48/56	CFP	4–29
4040234	PK	3	HSIP	3-62	4040167	WF	208	CFP	4-59
4040152	PM	64	TQFP	2-127	4040227	WG	240	CFP	4-61
4040135	PN	80.	TQFP	2-129	4040168	WH	240	CFP	4–62
4040016	PP	208	QFP	2–97	4081525	WK	240	CFP	4–63
4040284	PPB	208	HQFP	2–113	4081526	WM	240	CFP	4–64
4040286	PPE	208	HQFP	2-114				-	



SEMICONDUCTOR PACKAGING TRENDS

Packaging bridges the gap between silicon and systems. With this new definition of semiconductor packaging, it is obvious that the continuing compression of the life cycle of end equipment means reduced time-to-market of semiconductor components. It is, therefore, timely that this updated version of the TI Semiconductor Group *Package Outlines Reference Guide* be issued now. It also calls for a brief overview of the packaging trends that will highlight TI's emphasis on concurrent technology development, aiming at just-in-time technology. Furthermore, it will highlight what semiconductor assembly and packaging can contribute to harmonization of processes and semiconductor products and to mastering the design challenges and the custom system needs of the future.

To illustrate the overall trend in semiconductor products (see Figure 1 – Packaging Roadmap), the composite parameter *package performance density* is used to arrange the sequence of products in time. The contributions that add up to the package performance density and their relative weights are listed on the right hand side of the illustration. Besides form factors such as lead count, package size, thickness, and the footprint, the list also contains prominent performance characteristics such as power dissipation and signal frequency. Last, but definitely not least, a column marks the cost sensitivity of a package. It is well known that many factors enter into cost, notably manufacturing volume, cost of chip and piece parts such as lead frame and materials, production process complexity, and reliability requirements.

This book is a compilation of drawings for all standard TI packages, but it also shows the customer TI's high standards of technology and manufacturing flexibility that permit the production of specialty product beyond the scope of this book.

The dual-in-line packages (DIPs) that were dominant in the 1970s retained their pre-eminence through most of the 1980s. Their sturdy leads are well suited for through-hole board assembly but are limited in the number that can be accommodated without unduly elongating the package. Consequently, higher pin counts for through-hole mounting applications had to be arranged in a two-dimensional pattern, resulting in the so-called pin-grid arrays (PGAs). There are, however, practical limitations. Finer pitch sizes result in thinner pins, which are more sensitive to handling and to insertion by machines into sockets and are generally more difficult to straighten. The trend, therefore, leads to ball grid arrays, in which the pins have shrunk to contact balls. They are slowly gaining wider acceptance; cost and reliability issues need to be considered carefully.

The conversion of through-hole packages to surface-mount packages has accelerated each year since the mid 1980s but has not moved quite as quickly as predicted earlier because it took longer than anticipated for users to transform the logistics, especially for pick-and-place machines and solder reflow facilities. It is important to note that surface-mount packages have been accompanied by a much reduced pitch of their leads. This trend is continuing for both gull wing shaped leads and J-shaped leads. With its leadframe producing factory and superior preplated lead finishing technology, Texas Instruments has the capability of producing high lead-count semiconductor devices.

Tape automated bonding (TAB) is the preferred technology for assembling chips that need from 300 to 1000 connections and beyond. While TAB presently is still restricted to bonding the chip periphery, the alternative technology of flip-chip assembly uses metallic bumps distributed two-dimensionally over the chip area. Both TAB and flip-chip assembly are being pursued intensively by Texas Instruments to achieve higher numbers of interconnections to the outside world.

In contrast, the approach of limiting the number of outside connections to a modest number (about 50 to 150) has only recently received attention. This need is now under accelerated investigation by several industrial research centers for the electrical and thermal performance advantages and potential low cost. QFP's currently support up to 304 pins, but this will not meet future needs. This aproach involves combining several active and passive devices (with or without individual housing) on a substrate with customized interconnection and then encapsulating this assembled subsystem or system as a new customized product. So-called single-in-line package (SIP) with SOJ memory devices surface mounted on a substrate with double layered interconnect have been manufactured by TI for almost 10 years. An extension of SIP is the slim memory card. The multichip module, which TI produced for special Japanese customers, represents a plastic version of the earlier ceramic hybrid systems still manufactured preferentially for military customers.



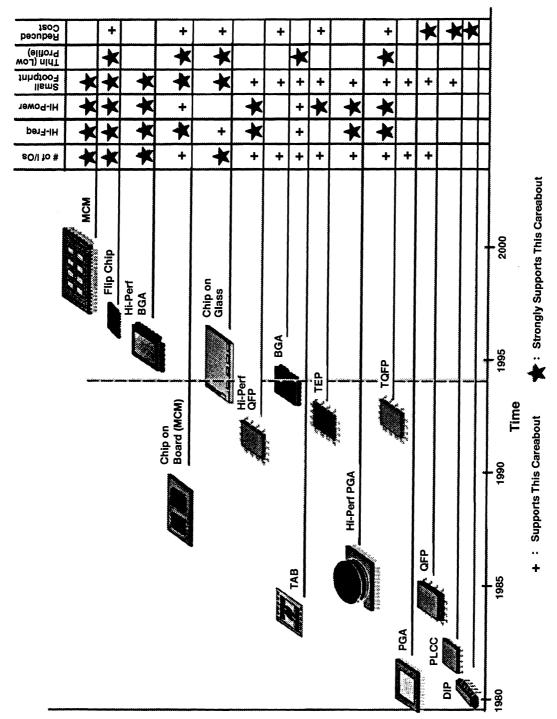


Figure 1. Packaging Roadmap

Package Evolution

The best electrical and perhaps thermal performances and the most flexible assembly are expected from flip-chip technology (by combining, for instance, digital and analog chips or silicon and gallium arsenide [GaAs] materials). This technology also promises the capability for true three-dimensional assembly, which produces customized systems at optimum packaging density. At the present time vertical assemblies are introduced by ZIPs, which are inserted into or surface mounted on boards. The trend of multichip modules (MCM) is expected to continue beyond the year 2000, with applications pervasive in computer, automotive, telecommunications, and consumer products.

Through-Hole and Surface-Mount Assembly

Dual-in-Line Packages. Plastic DIPs still account for close to 50% of the world semiconductor output. For almost two decades, they have been and still are the work horse of the high-volume and general purpose logic products. They cover only a restricted number of pins (8 to 64), package dimensions, and types of packages.

The leadframes are made of copper or Alloy 42. The lead finish is either solder applied by a dipping or plating process or palladium[†]. Because DIPs are used for relatively low-cost chips, there is continued pressure to implement cost reduction. This endeavor drives material, labor, and yield loss savings as well as the potential conversion to copper wire bonding from present gold wire bonding.

Surface-Mount Packages. In the early 1980s, a trend started that is still accelerating today: to design new semiconductor products for board attach by surface-mount technology (SMT) rather than by through-hole soldering. The reason is an increase of board density and a decrease in board cost by a factor of 3 to 5 compared to through-hole assembly. This significant savings justified the investment by users in new pick-and-place machinery and solder reflow equipment.

Gull wing shaped leads offer the advantage of easy lead inspection but are sensitive to transport and socket insertion. They require, therefore, shipment in trays rather than on the traditional rails. J-shaped leads, on the other hand, are more robust in handling but are more difficult to inspect after board attach.

In addition to the economic advantage, surface-mount technology offers a number of technical advantages for device manufacturing as well as board assembly. Consequently, it is projected to be the overwhelmingly dominant packaging and assembly technology in the second half of this decade. For a more detailed discussion of the packaging trends, it is, therefore, sufficient to consider these trends in the light of surface-mount technology. The major trends in assembly and packaging are as follows:

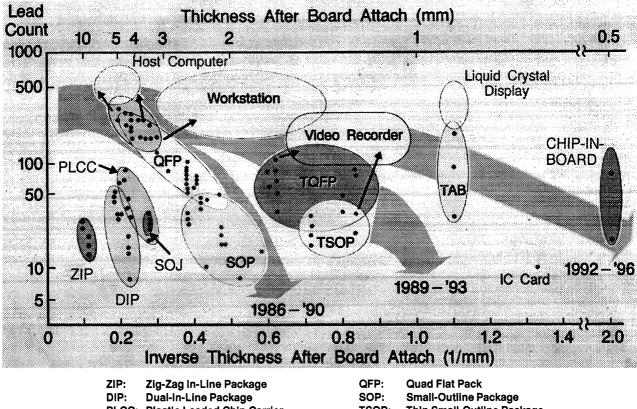
- A push towards higher lead counts
- A trend toward smaller packages (reduction of two dimensions)
- A combination of the two trends above resulting in finer lead pitch
- An additional trend towards thinner packages (reduction of the third dimension)
- A need to harmonize chip characteristics with package characteristics to end up with the desired device parameters (especially electrical, thermal and reliability performance)
- A need to tolerate higher power density and dissipate more heat
- A demand for drastically higher reliability, especially for package integrity and minimum stress
- A drive towards time-to-market

[†] Palladium is used on lead frames (dips and surface-mount packages) to eliminate chemically aggressive fluxes used during solder finishing as well as eliminating lead from the assembly process.



Trend Towards Higher Lead Counts and Thinner Packages

Figure 2 plots the lead count (on a logarithmic scale) versus the assembled height of the semiconductor device over the assembly board (abscissa is linear for inverse thickness after board attach). The dots representing products in the TI device portfolio clearly group into major device families. The families arrange themselves to an evolutionary sequence in time, stretching to the end of this decade.



DIP: Dual-In-Line Package SOP: Small-Outline Package PLCC: Plastic Leaded Chip Carrier TSOP: Thin Small-Outline Package PGA: Pin Grid Array TQFP: Thin Quad Flat Package SOJ: Small-Outline J-Leaded Package TAB: Tape Automated Bonding

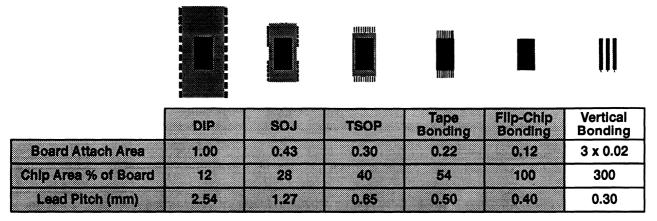
Figure 2. Applications Drive Lead Count

The applications (host computer, workstation, etc.) listed in Figure 2 symbolize the lead count needs of major device systems. They are grouped according to the thickness of the device boards, with the devices of liquid crystal display drivers occupying less than 1 mm height over the board. The remarkable feature of Figure 2 is the observation that none of the semiconductor device families satisfy the lead count needs of the application systems. Consequently, a strong and persistent push is currently exerted, indicated by the arrows, to drive the device families to ever more numerous connections to the outside world. This push is expected to persist for the next several years. It will be highlighted in a later section that surface-mount devices are particularly well suited to respond to the drive towards higher lead counts.

Furthermore, Figure 2 shows a few product families with extraordinarily thin device body and thus height after board attach. Tape automated bonding enables a reduction of the device thickness to less than 1 mm height over the board. As the final stage of this development, unencapsulated chips allow a chip-in-board assembly with the overall board thickness not more than the chip itself, i.e., less than 0.5 mm.



With surface-mount technology offering design and process flexibility to reduce the package size, strong economic pressure developed several years ago to shrink package sizes so that valuable board area is saved in assembly. The board utilization gains achievable are shown in Figure 3 by following the package shrinkage of a 1M/4M DRAM chip. The memory chip encapsulated in a 20-pin dual-in-line package (DIP) utilizes only 12% of the board area consumed by the package area, while for a thin small-outline package (TSOP) the utilization improved to 40% of the board area needed for the package. In flip-chip bonding, all the board area consumed is used by the chip itself; this technology represents optimum (100%) board utilization. It requires the trick of positioning the chips on their small sides to achieve several factors (300% and up) higher board usage for chip function per given chip area at flat assembly. Consequently, vertical assembly will be needed for future economic gains in valuable board area.



Package-Related Failure Mechanisms									
Increasing Importance	Diminishing Importance								
 Package Integrity 	Stress in Chip								
 Popcorn Effect 	Bond Chip-Out								
Material Fatigue/Crack	Metallization Shifts								
Electrical and Thermal Fallu	re Corrosion								

Figure 3. Smaller Packages Demand Less Plastic With No Degradation of Reliability

It is important to realize the nonnegotiable precondition underlying this package shrinkage: the reliability of the device must not degrade. On the contrary, much effort is being expended by the industry to improve the reliability for less or even no plastic material around the chip. As listed in Figure 3, emphasis is placed on enhanced package integrity by eliminating separation of molding compound from chip and leadframe (popcorn effect), enhancing adhesion, suppressing material fatigue or cracking, and avoiding failures caused by electrical, thermal or moisture effects. In all these endeavors, Texas Instruments has been and is a leader in the industry, as the remarkably improved reliability data for accelerated testing of semiconductor surface-mount products has demonstrated.

To ensure this pivotal adhesion and moisture/temperature robustness, several product-type-specific materials/process criteria and design features have proven successful.

GENERAL INFORMATION

 Molding compounds have to be selected and routinely controlled to maximize chemical adhesion and strain/stress inner energy, especially at elevated temperature

Quantitative tests are:

- Lead pull force, to determine how lead design and mold compound affects adhesion
- Strain/stress diagram of rods of polymerized molding compound as a function of the temperature
- Leadframe surfaces have to be clean and unoxidized.
- For leadframes with large chip pads, the bottom side should exhibit texturing, e.g., dimples or grooves, to allow mechanical anchoring of the molding material.
- Polyimide layers on the chip surface and on the bottom of the leadframe may enhance chemical adhesion to molding compounds.

In order to retain perfect adhesion after temperature cycling of the device (especially after water absorption by the plastic in steam exposure and preconditioning), the following features have proven helpful.

- The package has to be designed so that the plastic shows equal thickness above the chip and below the leadframe. This will produce equal compressive forces of the molding compound after polymerization.
- The coefficients of thermal expansion (CTE) of all parts should approach that of the molding material (20 ±8 ppm) if cracking of the plastic is a risk. Usually this drives a requirement for copper leadframe material.
- CTE should approach that of silicon (2 ppm) if fracturing of the silicon chip is a risk. Usually this drives a requirement for Alloy 42 leadframe material.
- Dry packing and shipping may be required for preventing moisture absorption in plastic.

Accelerated tests for product reliability include temperature cycling, usually –65°C to 150°C, and thermal shock after moisture preconditioning. In addition, dynamic simulation of molding compound flow helps to define the characteristics of void-free filling of narrow cavities, like the molds of 1-mm and 0.5-mm thin packages.

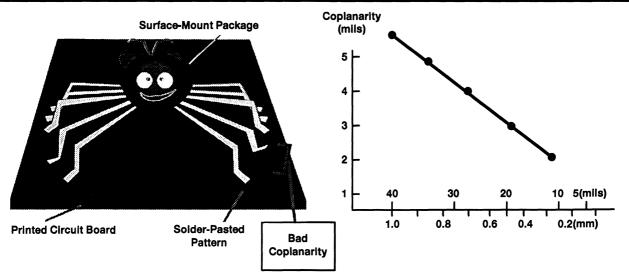
Lead Pitch and Coplanarity

As long as the pitch of the metallic leads remains at 0.50 mm, the device is still easy to handle. How does one perform surface mounting, though, if the lead pitch shrinks to 0.3 mm or even 0.15 mm as predicted by roadmaps in Japan? Handling, transport, and pick-and-place operations will be difficult without some method of support such as a flexible leadframe material underlying the leads. After all, these lead pitches are of the order of magnitude of the diameter of the human hair.

Another method for easing the handling of ultra-fine leads is the molded frame or molded ring approach. In this method, both the chip encapsulation and the robust support frame are molded in one process step. The metallic leads, bent around the frame, permit device testing and burn-in without touching the actual leads. They will be excised and formed right before assembly so that undisturbed leads will undergo the surface-mount soldering process without risk of coplanarity problems.

Figure 4 highlights the serious coplanarity problem. It also shows quantitative data, collected from large-scale users, on acceptable tolerances for lead coplanarity as a function lead pitch. As can be seen from this graph, a coplanarity of 2 mils, representing a tolerance window of ± 1 mil, is required for the lead pitch of 0.3 mm. Smaller pitch sizes will demand even tighter coplanarity windows – a tough feature to maintain.





TI Innovations

- Lead inspection system
- Lead conditioner system
- Palladium preplated leadframes
- Delayed-reflow solder paste

Figure 4. Lead Coplanarity of Surface-Mount Devices

Texas Instruments is offering several innovative approaches to support coplanarity solutions. An automated lead inspection system, available in the open market, measures the coplanarity quantitatively and determines whether any lead violates the allowed tolerance. The automated lead conditioner system corrects lead deviations by planarizing and straightening the leads. Both quality assurance systems are benchmark product lines.

Furthermore, preplating of nickel-plated copper leadframes with a noble metal, such as palladium, simplifies solder wetting and supports problem-free surface mounting. Finally, for customers who still use vapor phase reflow, a delayed-reflow solder paste will help establish thermal equilibrium and a more uniform solder flow. (The palladium preplated lead frame is discussed in more detail in the chapter titled Principles of Surface Mount.)

From the standpoint of maximum board utilization, it can be anticipated that flip-chip assembly will eventually be adopted. Figure 5 dramatizes the advantage of flip-chip assembly (100% board area used for functionality) when it is compared to more conventional board attach techniques. Even the almost flat-looping ribbon wedge technique still wastes some board space around the chip for affixing the outer wedge connections. In contrast, from a cost standpoint, no assembly technique is as inexpensive as wire bonding so far. This may change, though, if low-cost reflow bumps become available and gang bonding (all connections of a chip made at one time) can be performed reliably.

Lead-Over-Chip (LOC) Package

The new LOC package, developed jointly by Texas Instruments and Hitachi, Ltd. for use with the 16M DRAM and applied to shrink 4M and 64M DRAMs, increases the silicon area that can be enclosed in a standard package, minimizes on-chip noise, and makes the electrical characteristics of the leads more uniform.

These advances are made possible by a unique system for connecting the chip to the pins of the package. This new lead frame design features leads that are equal distance from one another and equal length. Nonuniform spacing of leads in today's typical small-outline J-lead (SOJ) package can allow as much as a 23% variation in lead-to-lead capacitance.



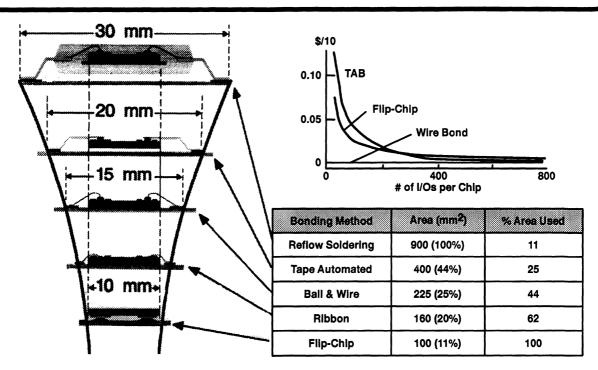


Figure 5. Board Usage Drives Interconnection Technology

The new package is a 28-/24-pin lead-on-chip with center bond (LOCCB) plastic SOJ (PSOJ). The 28-/24-pin SOJ package houses chips as large as 330×660 mils, conforms to JEDEC standards of 400×725 mils, and has dual power (V_{CC}) and ground (V_{SS}) pins. The LOC package also provides the most area-efficient chip design by minimizing the size of the on-chip power buses. The package leadframe itself routes power above the chip surface. Efficient use of the LOC package and effective power distribution require that the bond pads be in the chip's center rather than on its periphery (see Figure 6).

Voltage drops (IR) and difficult-to-manage thermal and mechanical stresses are foremost concerns. Thus the project makes wide use of the modeling and simulation strengths of both companies to design the LOCCB package. These joint efforts led to a 16M DRAM SOJ package exhibiting low-noise power distribution on-chip, less than 0.2 V drop, and less than 10 m Ω resistance and 6 nH inductance.

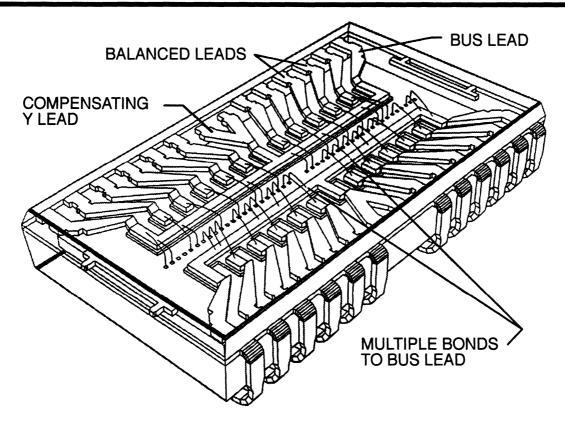


Figure 6. Lead-Over-Chip 16M DRAM Package

A unique balanced capacitance lead frame for maintaining uniform input pin capacitance is at the heart of the TI/Hitachi LOCCB design. All internal leads are equal distance from one another. A passive Y lead in the middle of the lead frame and on either side minimizes differences in pin-to-pin capacitance.

Two metal bus lines, integral to the lead frame structure, run parallel above the length of the chip. One links the dual V_{SS} pins located at the ends of the package while the other bus line links the corner dual V_{CC} pins on the other side of the chip. Multiple bonds are thus provided off the V_{SS} and V_{CC} bus lines to the circuit. With dual pins for each bus, resistance is reduced to less than 10 m Ω , effective inductance to about 6 nH, and electrical noise is less than 0.2 V.

General Information		1
Plastic Surface-Mount		2
Plastic Through-Hole		3
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Other Packages		6
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PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
SOIC (SMALL-OUTLINE IC)	8 8/14/16 16/20/24/28 20/24 28	JEDEC	DNA D DW DBQ DV	4040046 4040047 4040000 4073301 4040076	2-7 2-8 2-9 2-10 2-11
HSOIC (THERMALLY ENHANCED)	20 (In Development) 20 (In Development) 20 20	JEDEC	DWH DWP DWT DZA	4040096 4073226 4073228 4040060	2–12 2–13 2–14 2–15
SOP (SMALL-OUTLINE PACKAGE)	8 14/16/20/24 16 28 30 32 36 44 64	EIAJ	PS NS DWA DWB DF DBA DT DBJ DGH	4040063 4040062 4040061 4040259 4040038 4040211 4040264 4073325 4040068	2-16 2-17 2-18 2-19 2-20 2-21 2-22 2-23 2-24
HSOP (THERMALLY ENHANCED)	18 20 20 20(24) (In Development) 20 (In Development) 24	EIAJ	KL DSA DSB DBC DWS DSB	4040059 4040091 4040215-2 4040213 4073227 4040215-3	2-25 2-26 2-27 2-28 2-29 2-30
SSOP (SHRINK SOP)	28/48/56 14/16/20/24/28/30/38 48 60 64 70 80	JEDEC EIAJ	DL DB DP DQ DBE DT DBF	4040048 4040065 4040037 4040250 4040262 4040098 4040263	2–31 2–32 2–33 2–34 2–35 2–36 2–37
HSSOP (THERMALLY ENHANCED)	56 (In Development)	EIAJ	DBD	4040214	2–38
TSOP (THIN SOP)	20(26) 24(26) 28 32 32 40(44) 44 44(50) 50 64(70)	EIAJ	DGA DGA DGC DD DGC DGE DGE DGE DGE DGE DGJ DGE	4040265-2 4040265-3 4040260-2 4040097 4040260-3 4040070-2 4040070-3 4040070-4 4073300 4040070-5	2-39 2-40 2-41 2-42 2-43 2-44 2-45 2-46 2-47 2-48
TSSOP (THIN SHRINK SOP)	8/14/16/20/24/28 28/30/32/38 48/56 56 (In Development) 80 (In Development)	EIAJ	PW DA DGG DLT DBB	4040064 4040066 4040078 4073250 4040212	2–49 2–50 2–51 2–52 2–53
HTSSOP (THERMALLY ENHANCED)	20 (In Development)	EIAJ	PWP	4073225	2–54



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PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
SOJ (J-LEADED SOP)	20(26) 24(26) 24(28) 28 28 32	JEDEC	DJ DZ DZ DZ DZ	4040092-2 4040092-3 4040094-2 4040092-4 4040094-3 4040094-4	2–55 2–56 2–57 2–58 2–59 2–60
	40 42		DZ DZ	4040094-5 4040094-6	2–61 2–62
	34 50 54	EIAJ	DBG DZC DBG	4040256 4073275 4040257	2–63 2–64 2–65
PLCC (PLASTIC LEADED CHIP CARRIER)	18 22 32 20/28/44/52/68/84	RECTANGULAR SQUARE	FM FM FM FN	4040201-2 4040201-3 4040201-4 4040005	2–66 2–67 2–68 2–69
HPLCC (THERMALLY ENHANCED)	44		FNH	4040184	2–70
DFP/TFP (DUAL/TRIPLE FLAT PACKAGE)	48 60 64	14 × 20, t = 2.0 mm	FT FT FT	4040228-2 4040228-3 4040229	2–71 2–72 2–73
	76	14×20 , $t = 2.7 \text{ mm}$	PDR	4073181	2–74
QFP	44	10×10 , $t = 1.65 \text{ mm}$	PAD	4040276	2–75
(QUAD FLAT PACKAGE)	44 52	10 × 10, t = 2.0 mm	FR RC	4040159 4040151	2–76 2–77
	44 64	14 × 14, t = 2.7 mm	PE PF	4040099 4040067	2–78 2–79
	44	14×14 , $t = 2.0 \text{ mm}$	FS	4040160	2–80
	64 64 80 80 100 100 100 128	14 × 20, t = 2.7 mm	PAK PG PAF PH PAL PJ PJM PR	4040270 4040101 4040271 4040011 4040272 4040012 4040022 4040027	2-81 2-82 2-83 2-84 2-85 2-86 2-87 2-88
	80 100 128	14 × 20, t = 2.0 mm	FT FT PGJ	4040230-2 4040230-3 4040277	2–89 2–90 2–91
	144	20×20 , $t = 1.9 \text{ mm}$	PGG	4040222	2–92
	120 120 144/160 144/160 208 208 256	28 × 28, t = 3.5 mm	PB PBM PC PCM PP PPM PGH	4040014 4040023 4040015 4040024 4040016 4040025 4073173	2-93 2-94 2-95 2-96 2-97 2-98 2-99
	136	24 × 24, t = 4.9 mm	PAB	4040275	2-100
	240	32×32 , $t = 3.8 \text{ mm}$	PGC	4040026	2–101
BQFP (BUMPERED QFP)	304 100/132	40×40 , $t = 4.0 \text{ mm}$ 20×20 , $t = 3.8 \text{ mm}$	PDN PQ	4073180 4040045	2–102 2–103



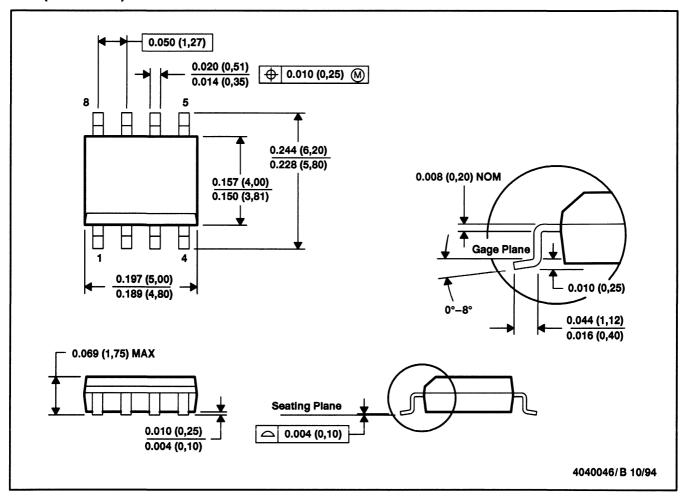
CONTENTS

PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
HQFP (THERMALLY ENHANCED)	128 (In Development) 100 100 100	14 × 20, t = 2.7 mm	PAC PJE PJG VH	4040274 4040123 4073174 4040177	2-104 2-105 2-106 2-107
	120 144/160 144/160 144/160 144/160 208 208 256	28 × 28, t = 3.5 mm	PBE PCD PCE PCY PCZ PPB PPE PGK	4040127 4040238 4040237 4040103 4040239 4040284 4040286 4073172	2-108 2-109 2-110 2-111 2-112 2-113 2-114 2-115
	240 240	32×32 , t = 3.8 mm	PGV PGY	4040247 4040245	2–116 2–117
	304	40×40 , $t = 3.8 \text{ mm}$	PDB	4040148	2-118
	100	BUMPERED	PJF	4040093	2-119
TQFP	32	5×5 , $t = 1.4 \text{ mm}$	PU	4040157	2–120
(THIN QFP)	32 48 64	7×7 , $t = 1.4 \text{ mm}$	VF PT PTA	4040172 4040052 4040216	2–121 2–122 2–123
	52 64	10 × 10, t = 1.0 mm	PAH PAG	4040281 4040282	2-124 2-125
	52 64	10×10 , $t = 1.4 \text{ mm}$	PBG PM	4040155 4040152	2–126 2–127
	80	12×12 , $t = 1.0 \text{ mm}$	PFC	4073177	2-128
	80 100	12 × 12, t = 1.4 mm	PN PFA	4040135 4073175	2–129 2–130
	100	14×14 , $t = 1.0 \text{ mm}$	PZT	4073179	2-131
	100 120 128	14×14 , $t = 1.4 \text{ mm}$	PZ PBK PBK	4040149 4040279-2 4040279-3	2-132 2-133 2-134
	144 144 176/184	20 × 20, t = 1.4 mm	PGD PGE PBL	4040156 4040147 4040154	2-135 2-136 2-137
	48	7×7 , $t = 1.0 \text{ mm}$	PFB	4073176	2-138
	176	24 × 24, t = 1.4 mm	PGF	4040134	2-139
HTQFP (THERMALLY ENHANCED)	64 (In Development)	10×10 , $t = 1.4 \text{ mm}$	PAJ	4040278	2–140
	100 100 120	14 × 14, t = 1.4 mm	VG PCA PCB	4040173 4040288 4040202	2–141 2–142 2–143



DNA (R-PDSO-G8)

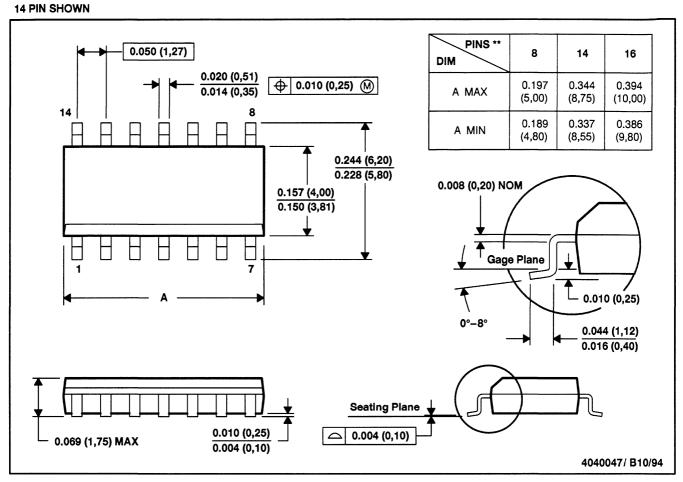
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad
- E. Falls within JEDEC MS-013

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

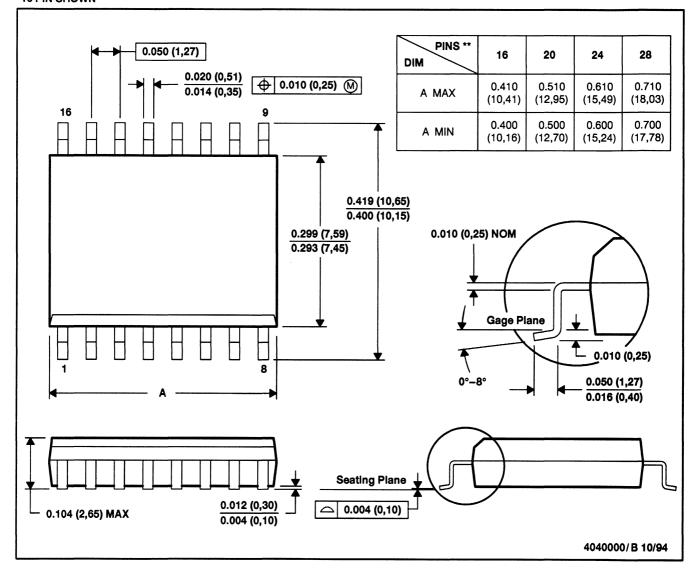


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad
- E. Falls within JEDEC MS-012

DW (R-PDSO-G**)

16 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

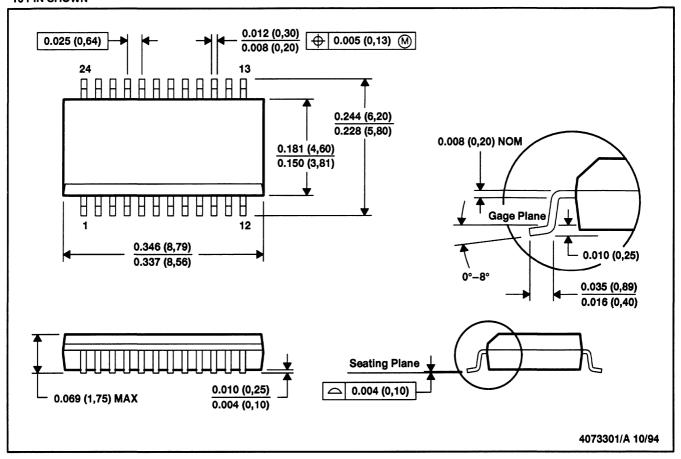


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

DBQ (R-PDSO-G20/24)

PLASTIC SMALL-OUTLINE PACKAGE

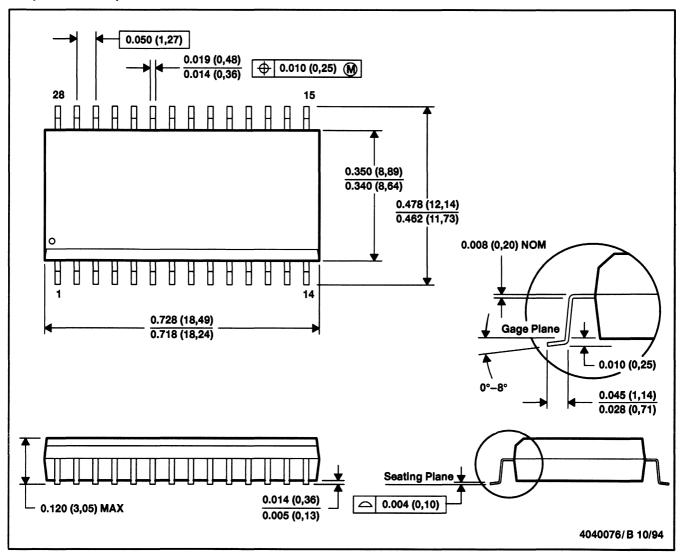
16 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-137

DV (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE

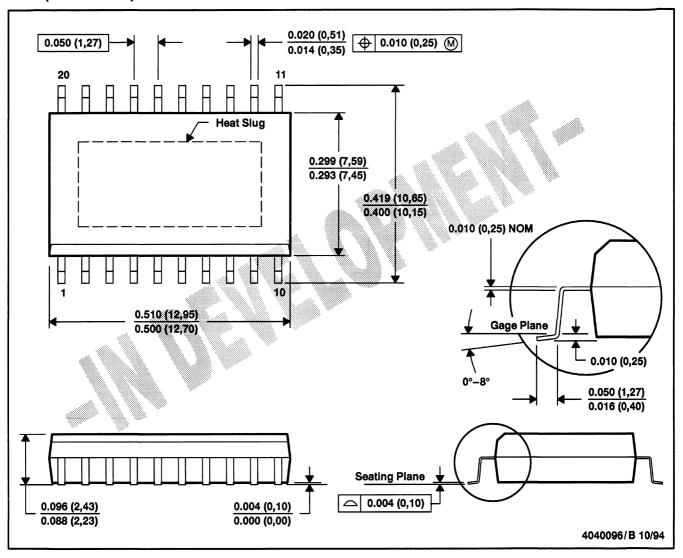


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

DWH (R-PDSO-G20)

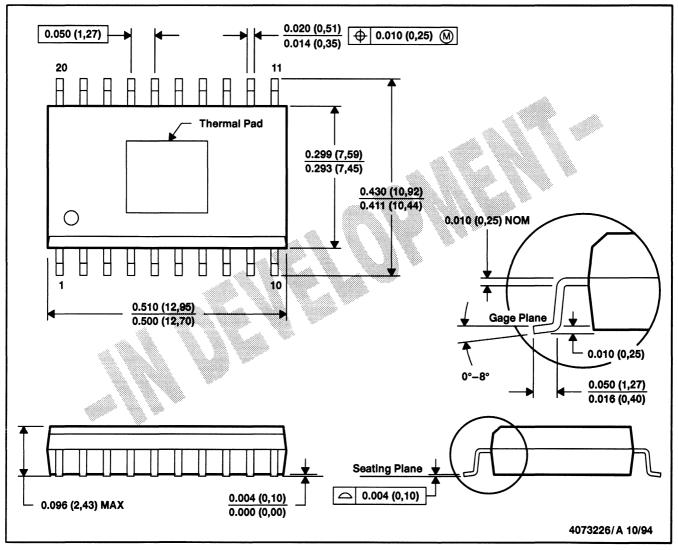
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.006 (0,15).
- D. Thermally enhanced molded plastic package with a heat slug (HSL) exposed on package bottom is electrically and thermally connected to the backside of the die and leads 3,4,7,8,12,13,16 and 17.

DWP (R-PDSO-G20)

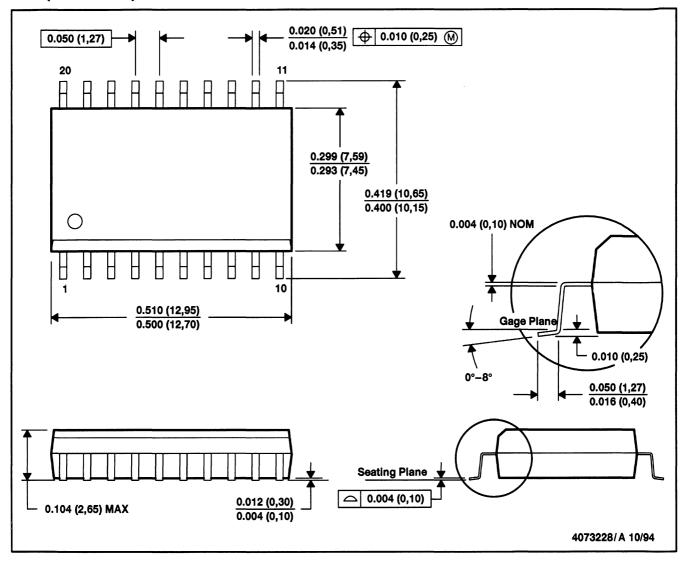
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. The solderable pad is electrically and thermally connected to the backside of the die and leads 1, 10, 11 and 20.

DWT (R-PDSO-G20)

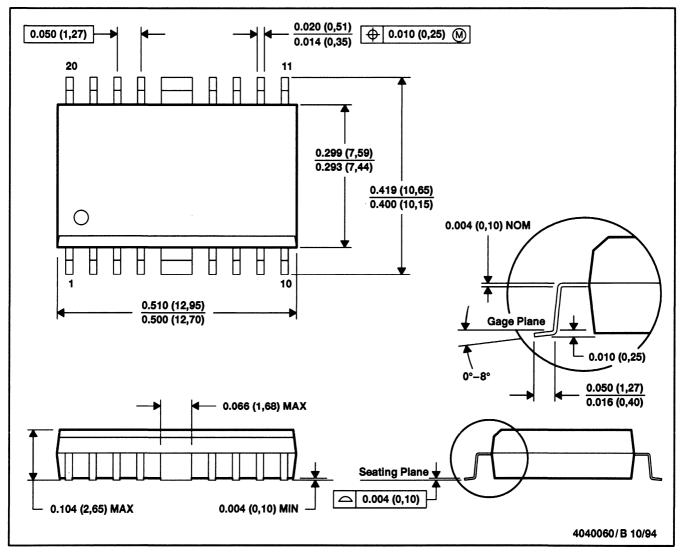
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with four center leads connected to die pad
- D. Falls within JEDEC MS-013

DZA (R-PDSO-G20)

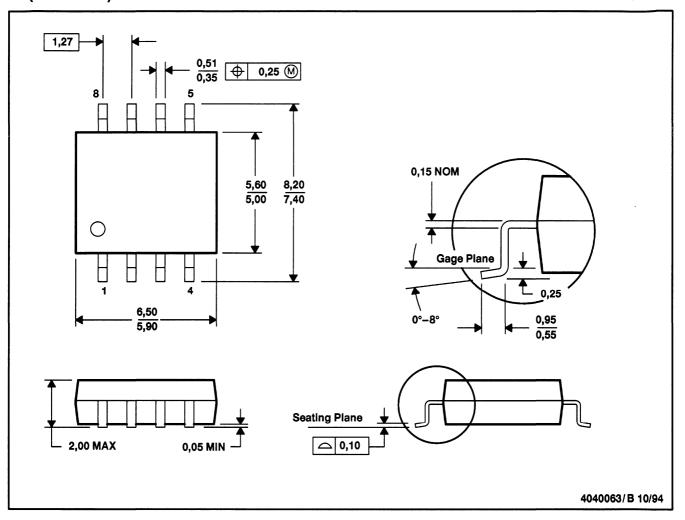
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.
- D. Thermally enhanced molded plastic package with a heatsink

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

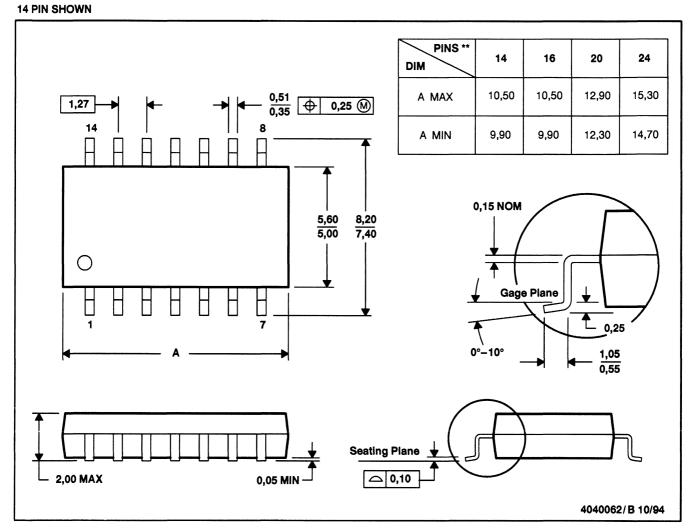


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

NS (R-PDSO-G**)

13 (h-PD30-G)

PLASTIC SMALL-OUTLINE PACKAGE



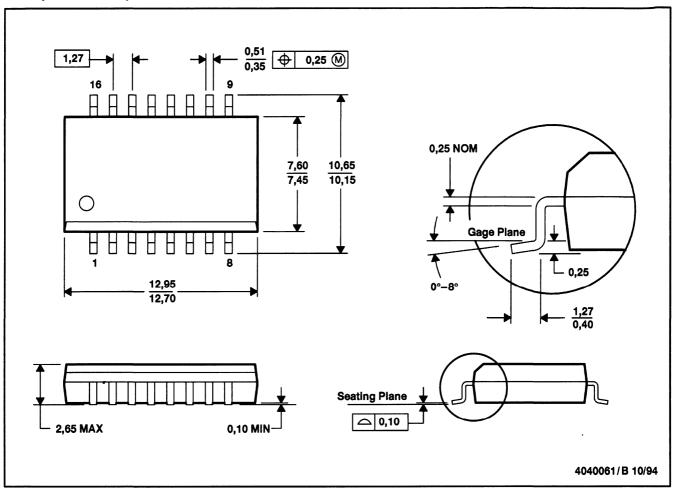
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DWA (R-PDSO-G16)

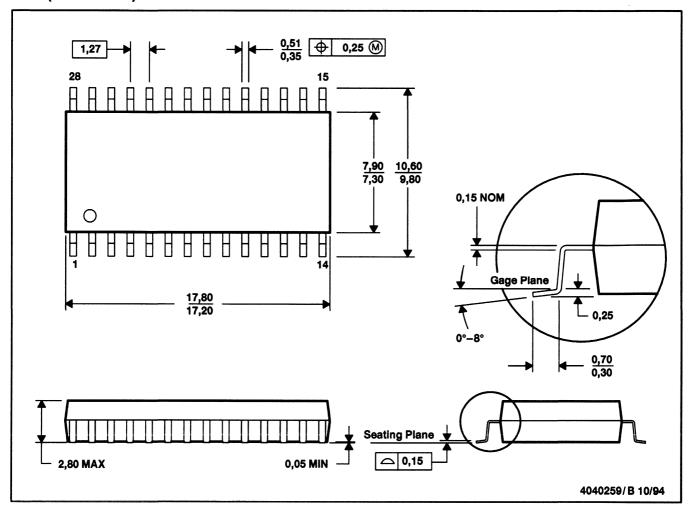
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DWB (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE

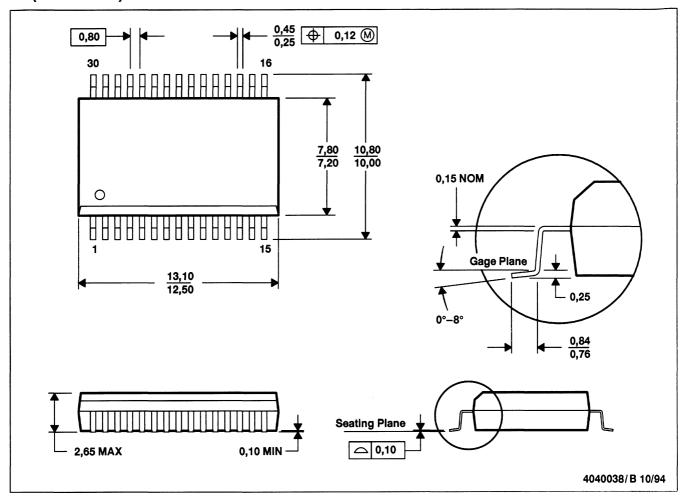


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.C. Body dimensions include mold flash or protrusion.

DF (R-PDSO-G30)

PLASTIC SMALL-OUTLINE PACKAGE

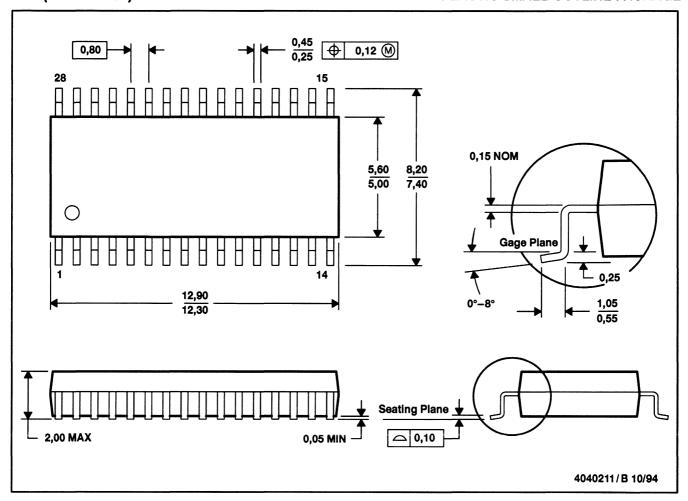


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

DBA (R-PDSO-G32)

PLASTIC SMALL-OUTLINE PACKAGE



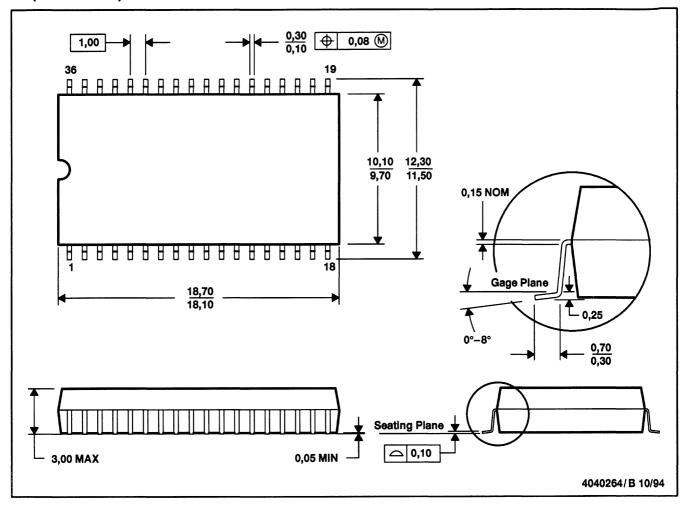
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DT (R-PDSO-G36)

PLASTIC SMALL-OUTLINE PACKAGE

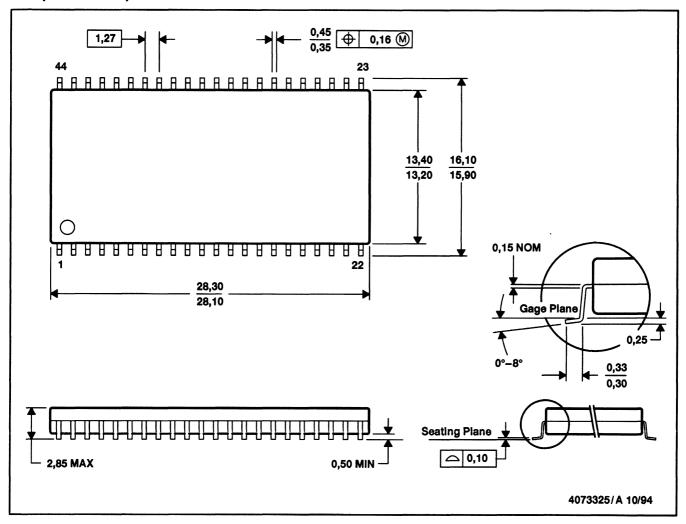


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

DBJ (R-PDSO-G44)

PLASTIC SMALL-OUTLINE PACKAGE



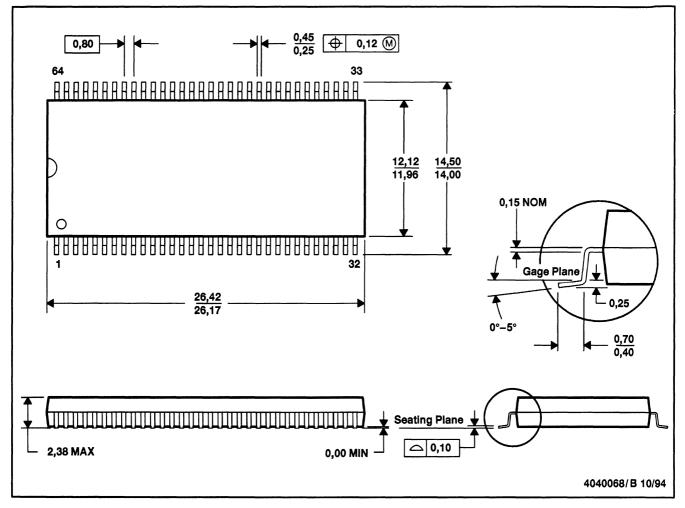
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

DGH (R-PDSO-G64)

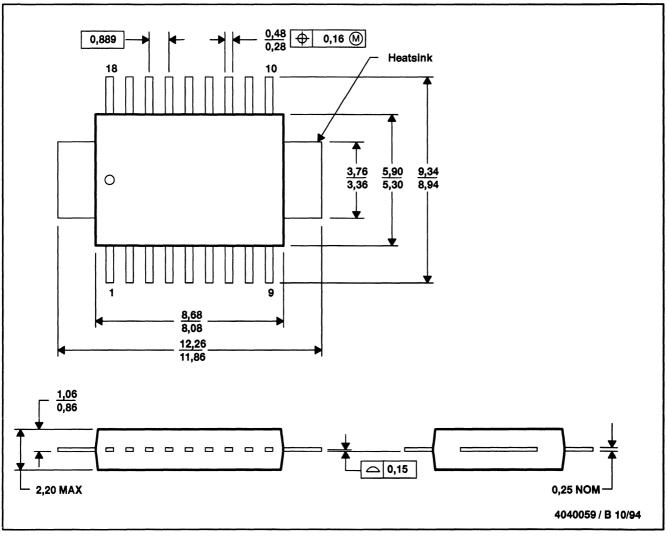
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold flash or protrusion. Maximum mold protrusion is 0,125.

KL (R-PDFP-F18)

PLASTIC SMALL-OUTLINE PACKAGE



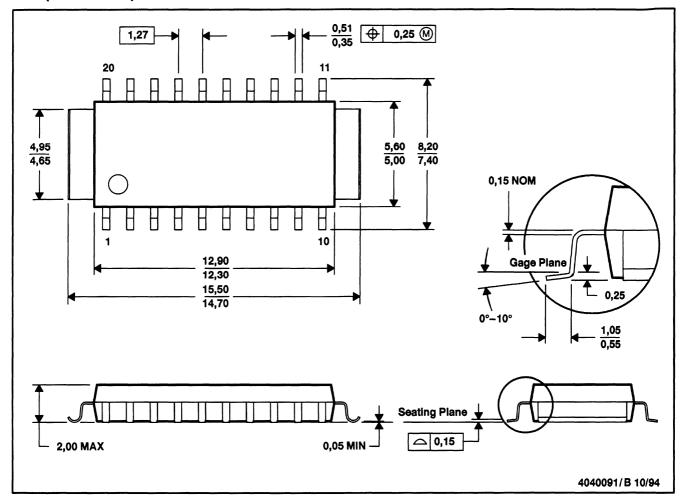
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Thermally enhanced molded plastic package with end tabs connected to die pad

DSA (R-PDSO-G20)

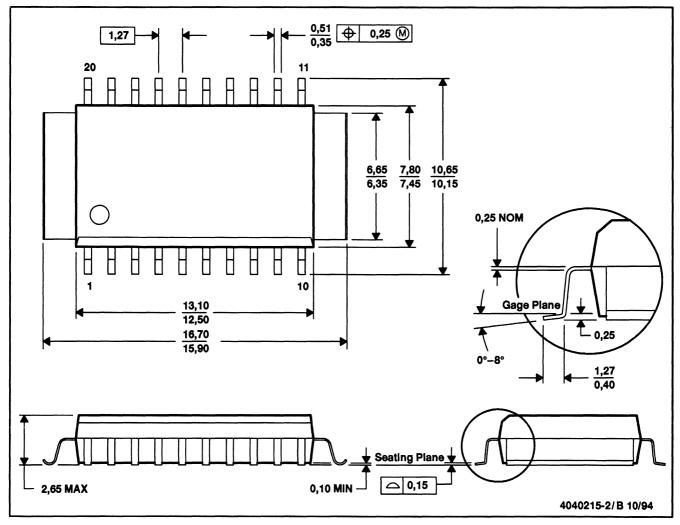
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Thermally enhanced molded plastic package with end tabs connected to die pad

DSB (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

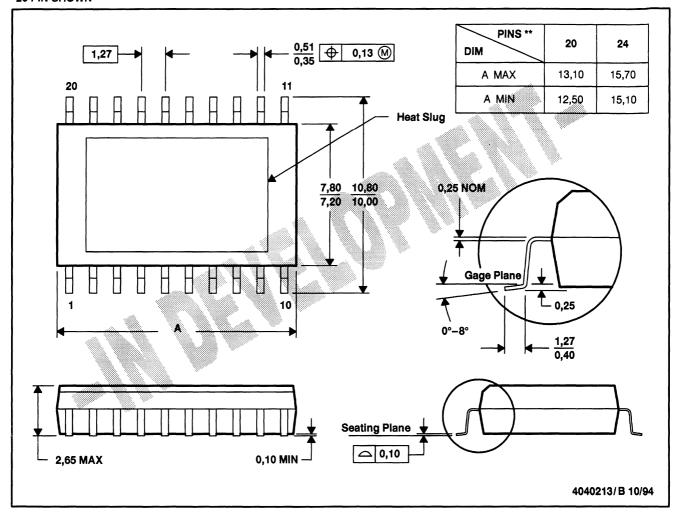


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Thermally enhanced molded plastic package with end tabs connected to die pad

DBC (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE (DIE-DOWN)

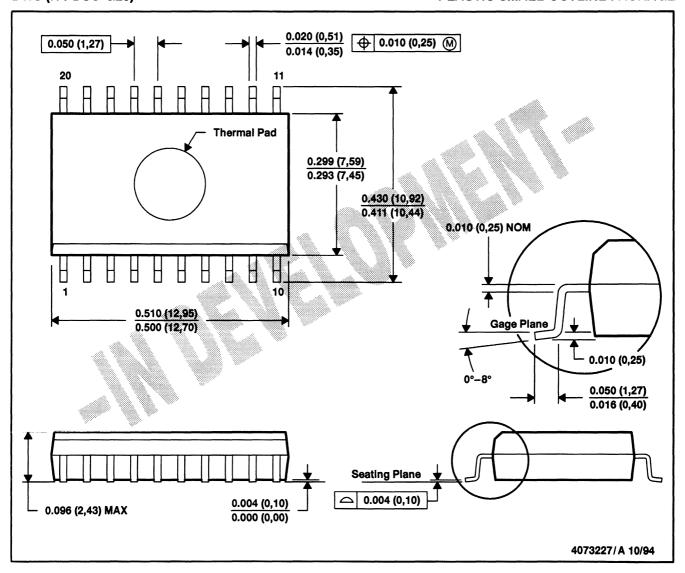
20 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)

DWS (R-PDSO-G20)

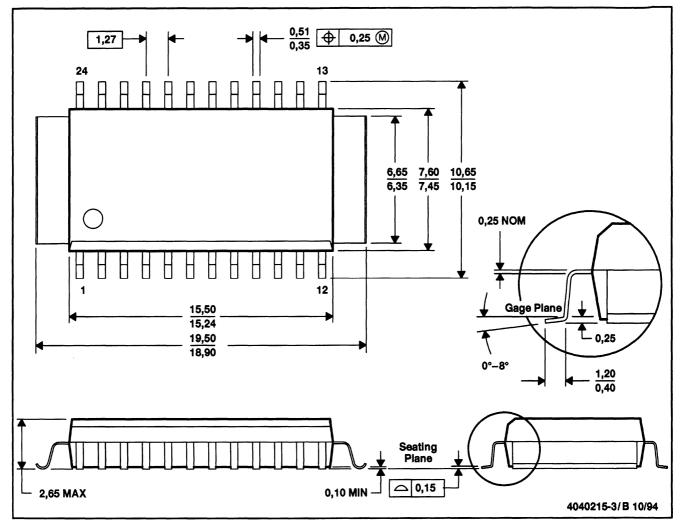
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. The thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. The solderable pad is electrically and thermally connected to the backside of the die and leads 1, 10, 11 and 20.

DSB (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

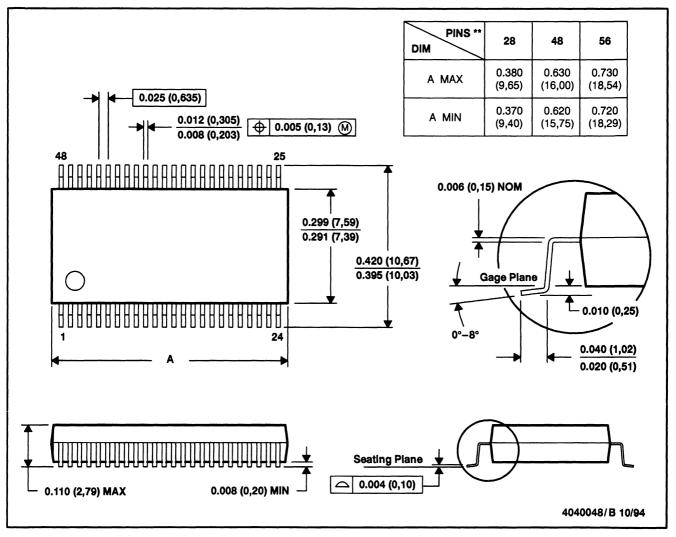


- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.
- D. Thermally enhanced molded plastic package with end tabs connected to die pad

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

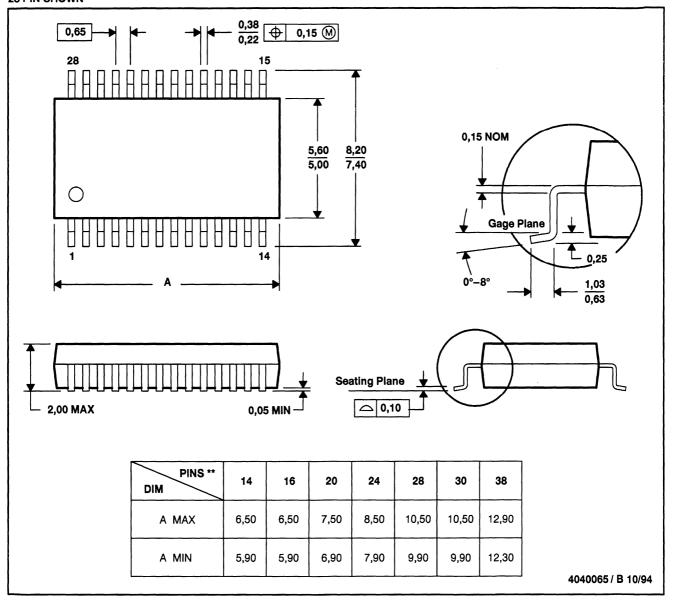
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

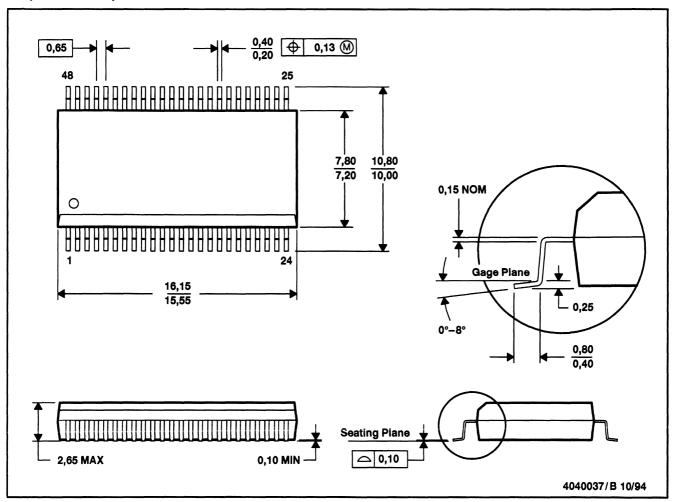
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D. Falls within JEDEC MO-150

DP (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



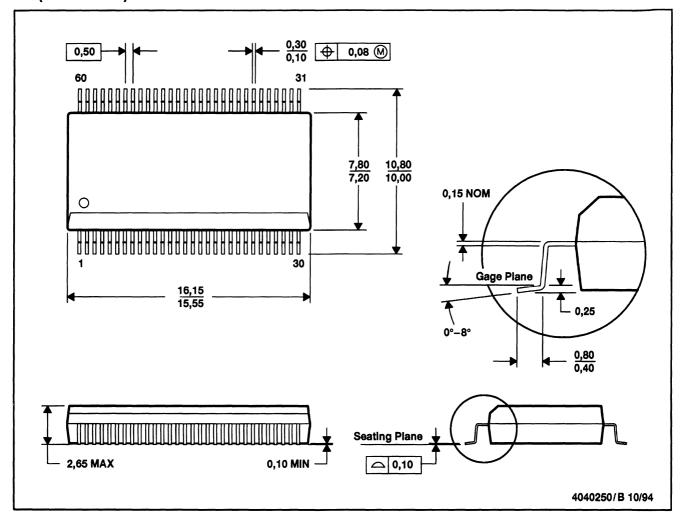
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

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DQ (R-PDSO-G60)

PLASTIC SMALL-OUTLINE PACKAGE

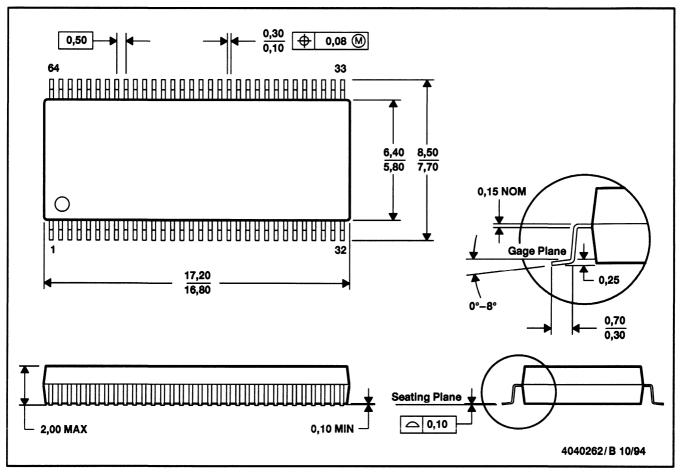


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

DBE (R-PDSO-G64)

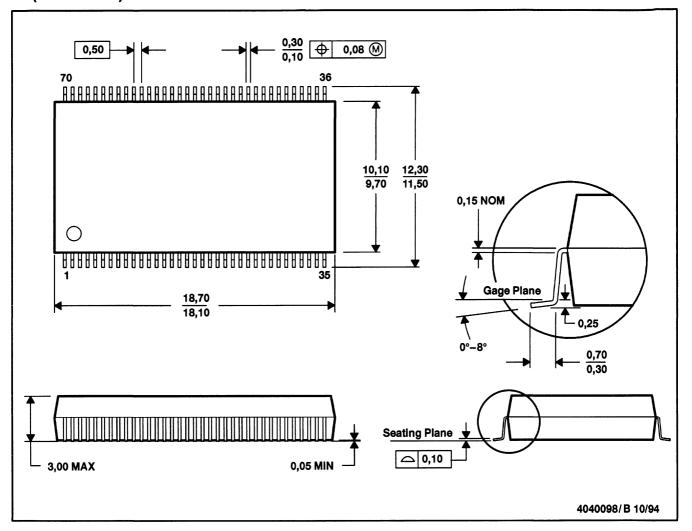
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

DT (R-PDSO-G70)

PLASTIC SMALL-OUTLINE PACKAGE

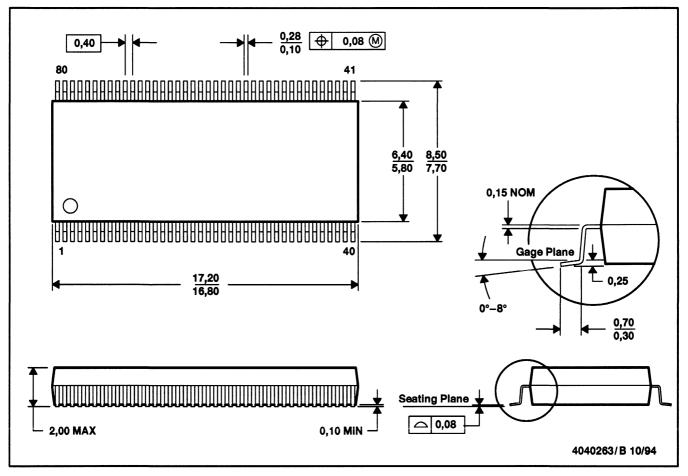


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

DBF (R-PDSO-G80)

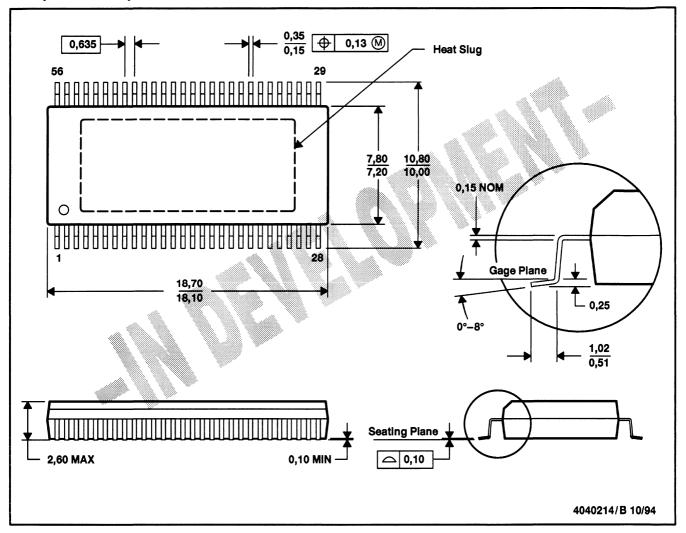
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DBD (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



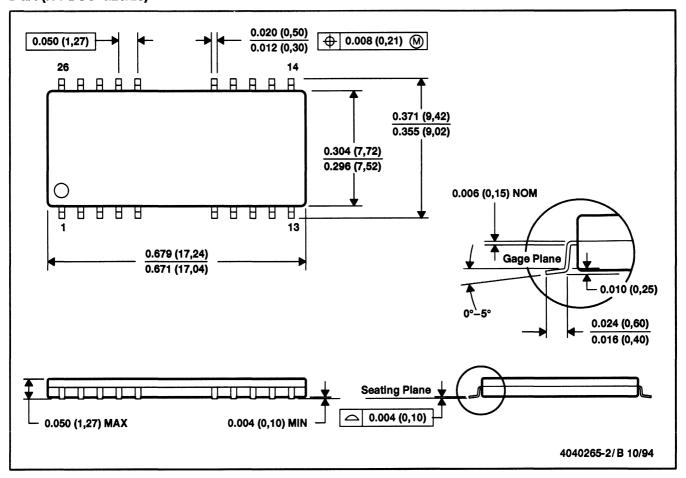
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Thermally enhanced molded plastic package with a heat slug (HSL) exposed on bottom of package

DGA (R-PDSO-G20/26)

PLASTIC SMALL-OUTLINE PACKAGE

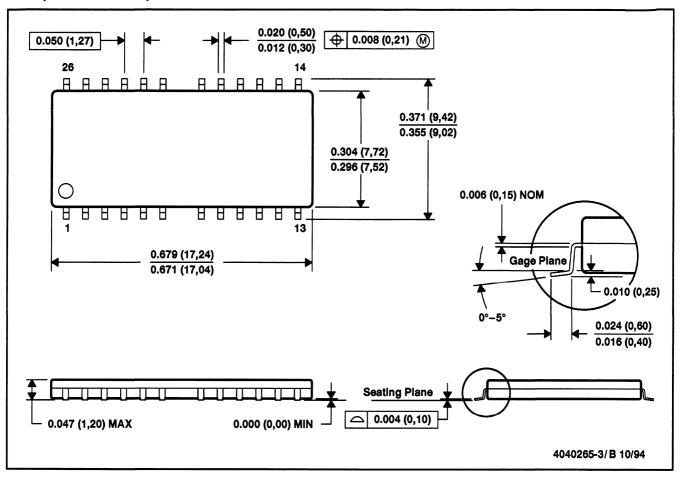


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DGA (R-PDSO-G24/26)

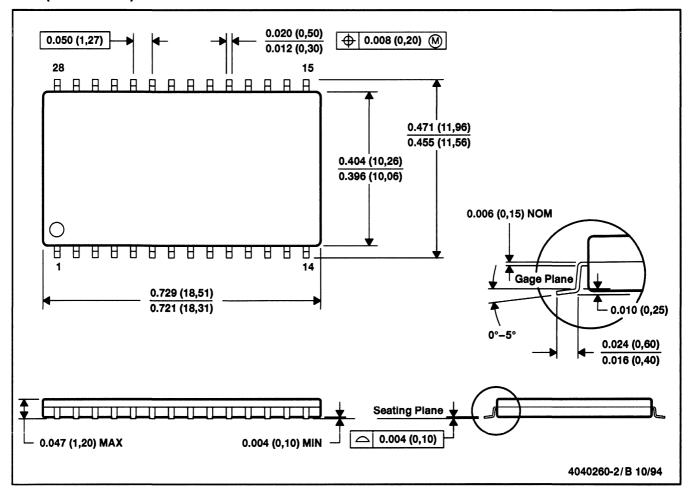
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DGC (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE

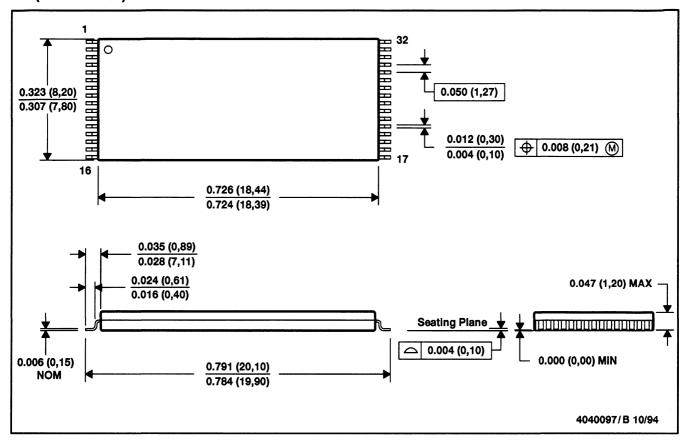


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

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DD (R-PDSO-G32)

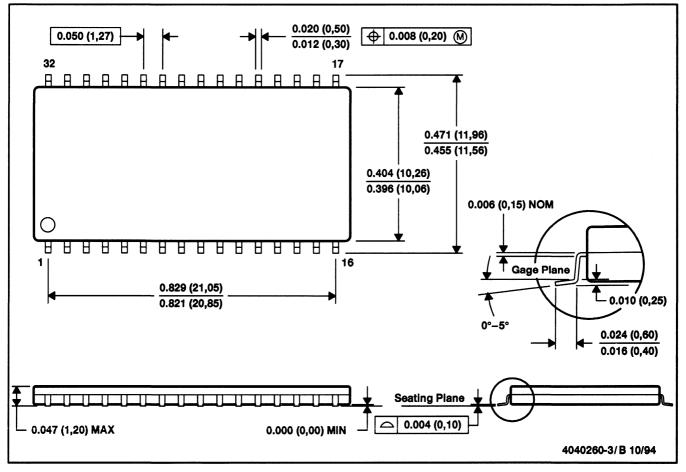
FLASH EPROM SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

DGC (R-PDSO-G32)

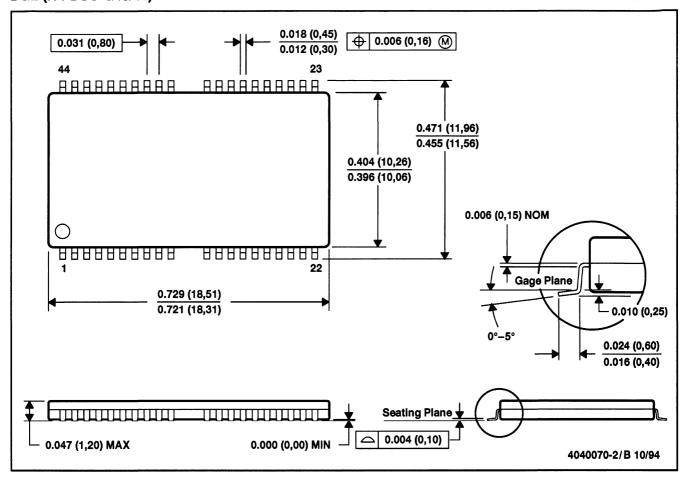
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DGE (R-PDSO-G40/44)

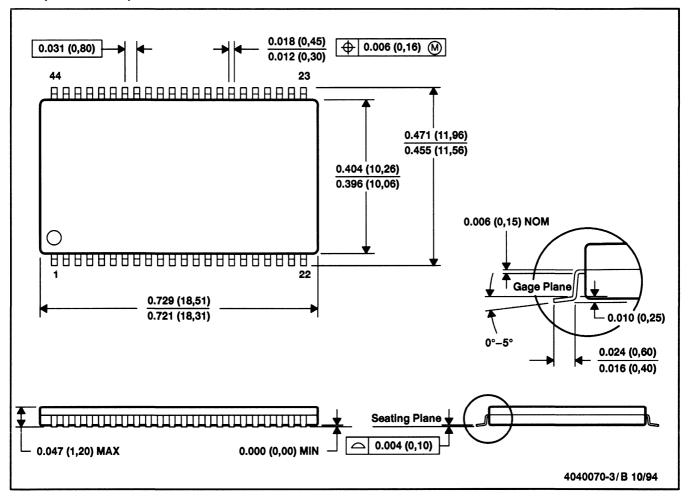
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DGE (R-PDSO-G44)

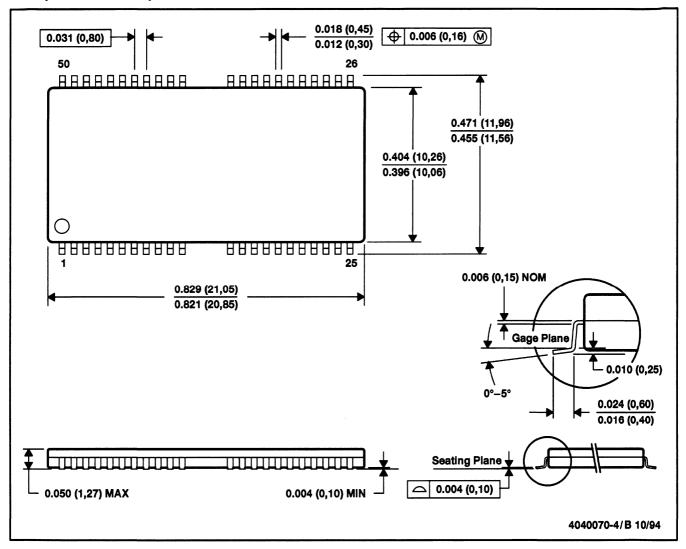
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.

DGE (R-PDSO-G44/50)

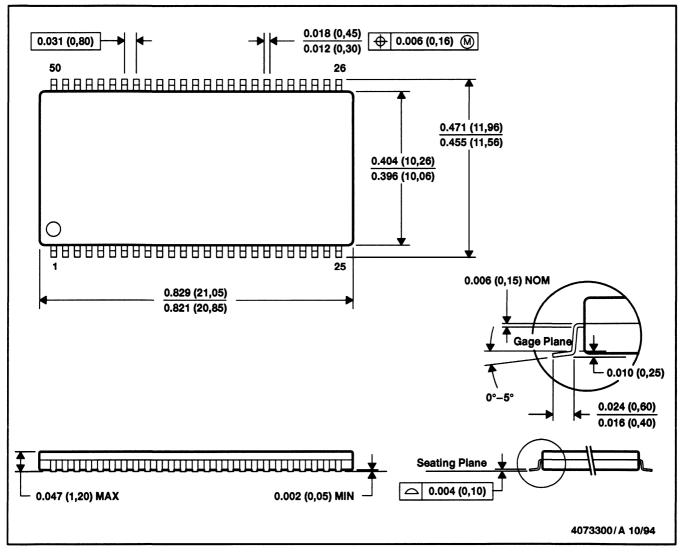
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

DGJ (R-PDSO-G50)

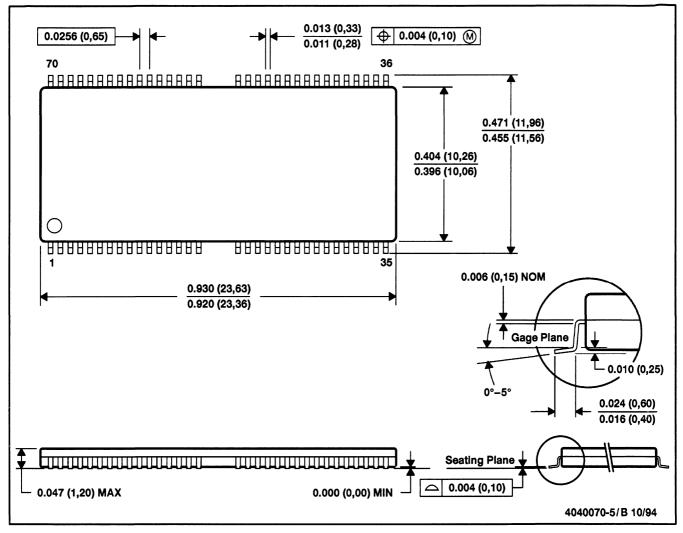
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Lead dimensions include plating thickness.

DGE (R-PDSO-G64/70)

PLASTIC SMALL-OUTLINE PACKAGE

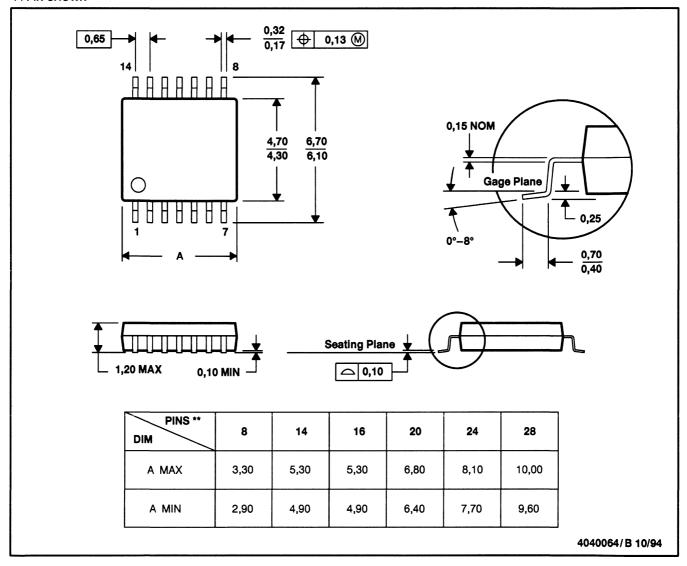


- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

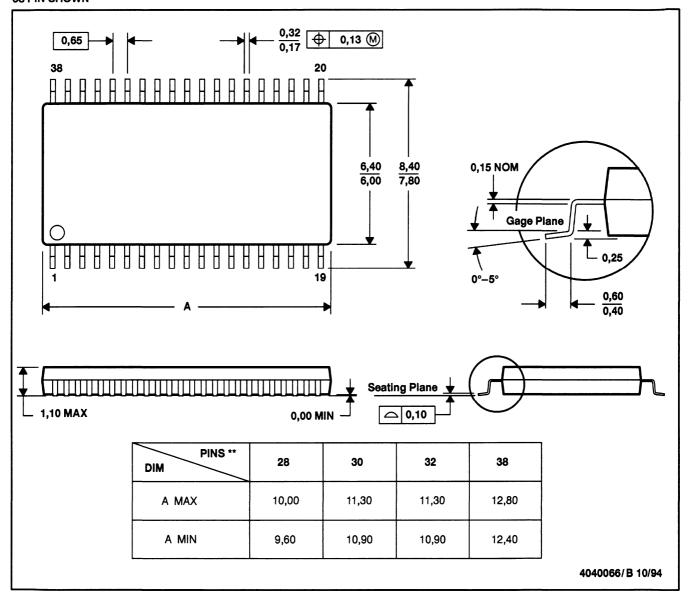
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DA (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

38 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

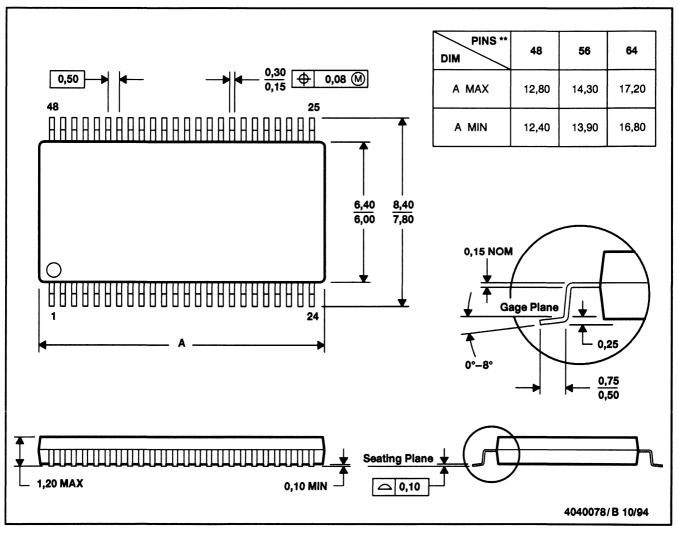
B. This drawing is subject to change without notice.

C. Body dimensions include mold flash or protrusion.

DGG (R-PDSO-G**)

48 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

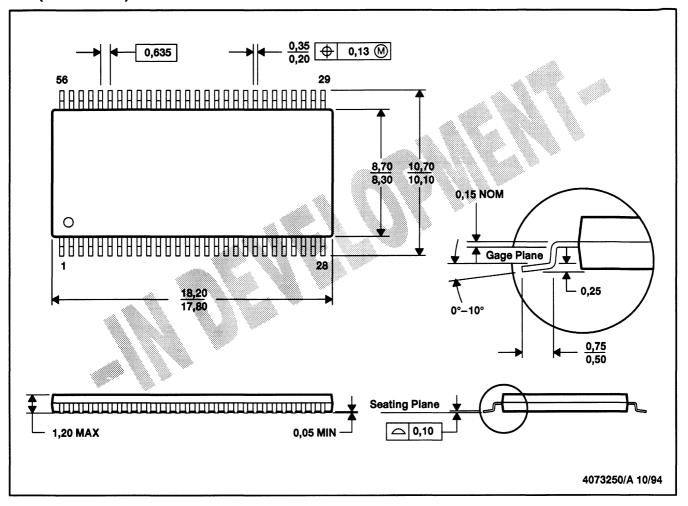


NOTES: A. All linear dimensions are in millimeters.

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DLT (R-PDSO-G56)

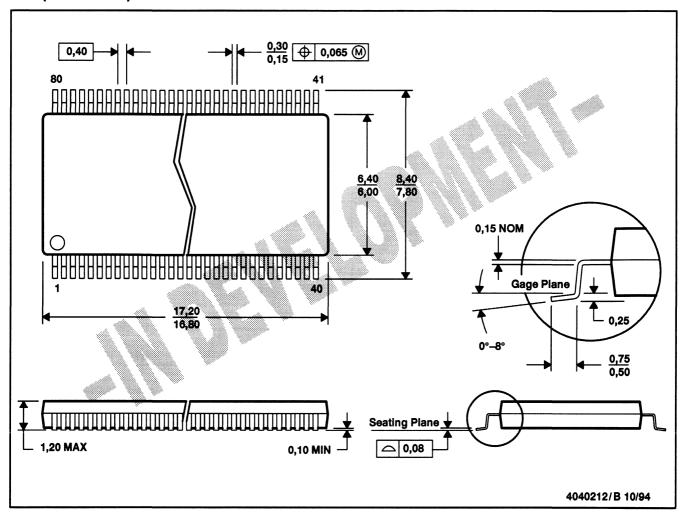
PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

DBB (R-PDSO-G80)

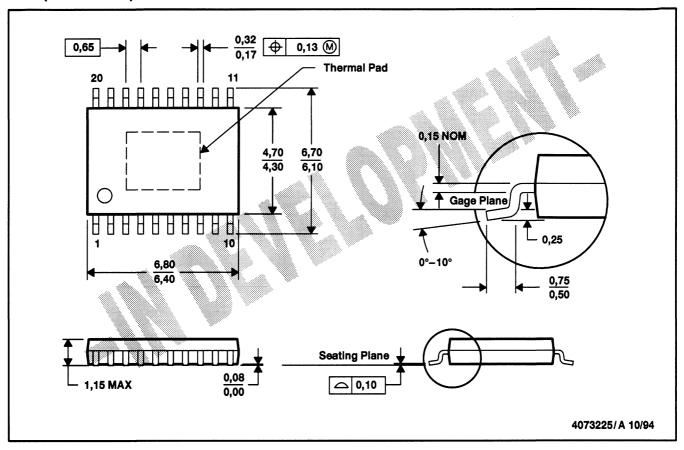
PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

PWP (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

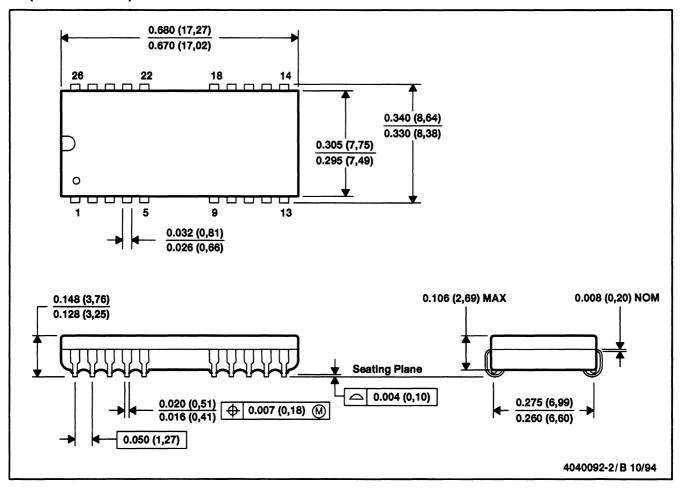


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. The solderable pad is electrically and thermally connected to the backside of the die and leads 1, 2, 9, 10, 11, 12, 19 and 20.

DJ (R-PDSO-J20/26)

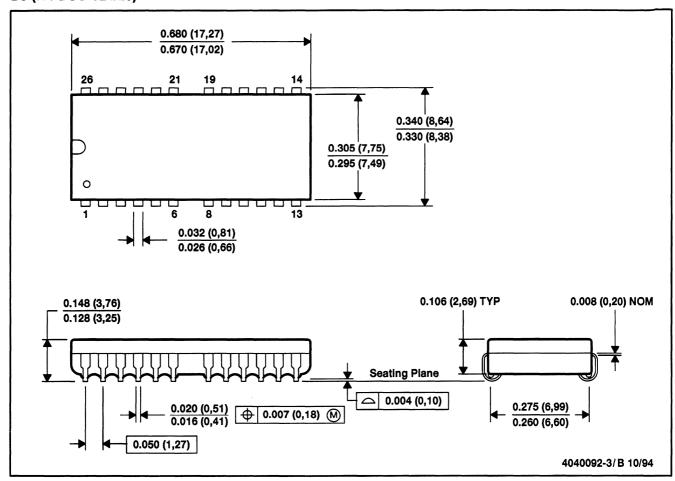
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DJ (R-PDSO-J24/26)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



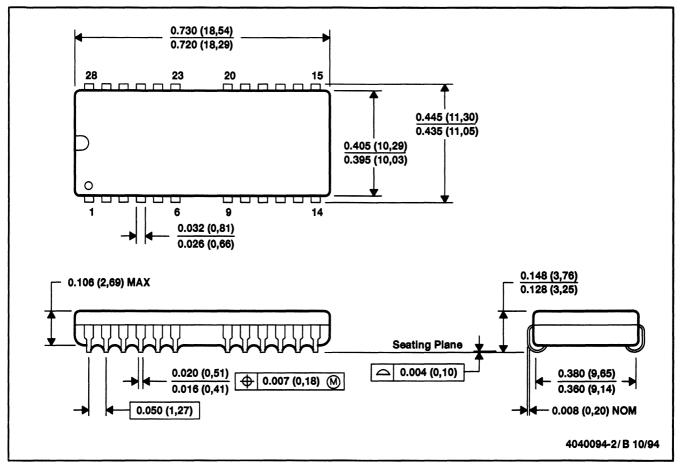
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DZ (R-PDSO-J24/28)

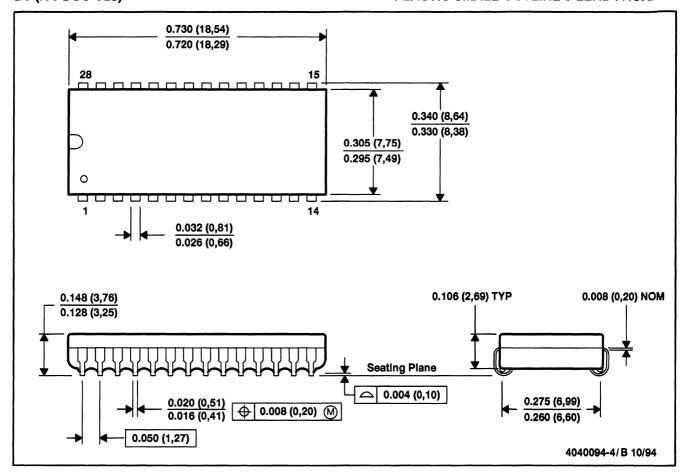
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DJ (R-PDSO-J28)

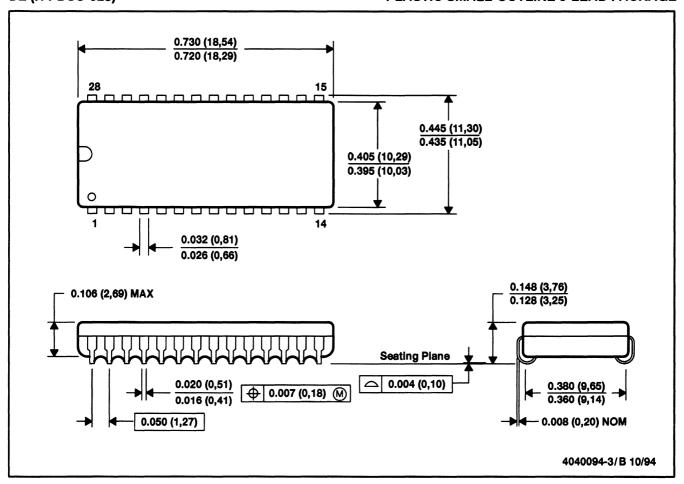
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DZ (R-PDSO-J28)

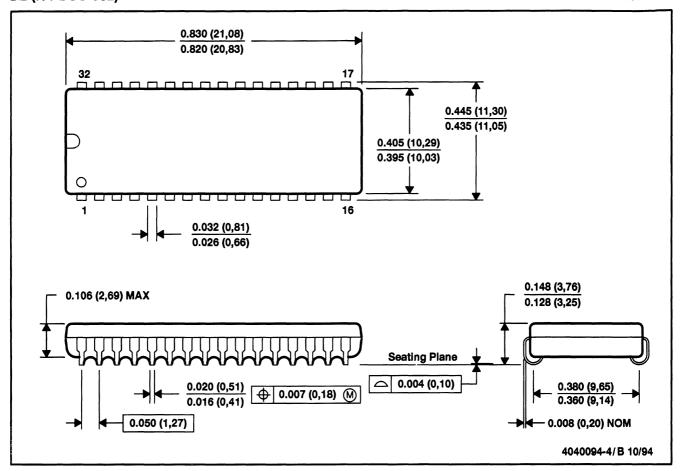
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DZ (R-PDSO-J32)

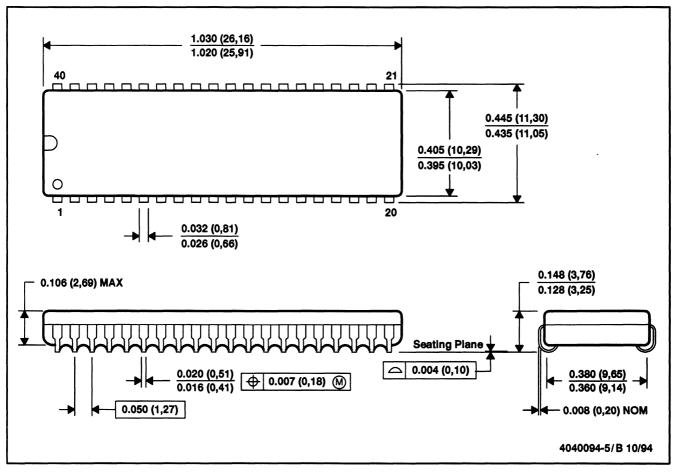
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DZ (R-PDSO-J40)

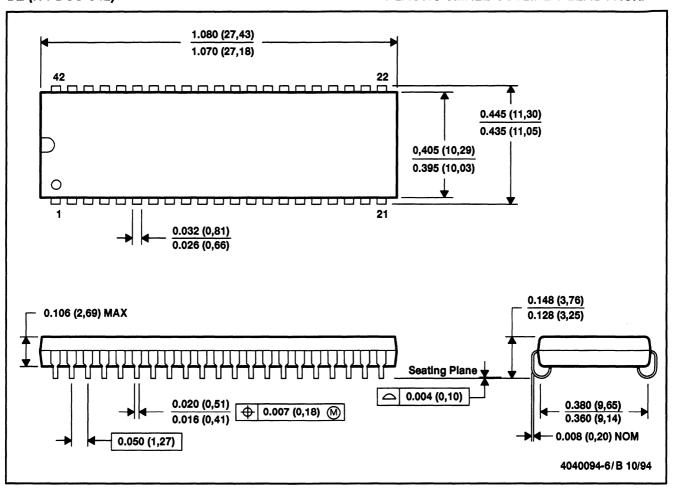
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DZ (R-PDSO-J42)

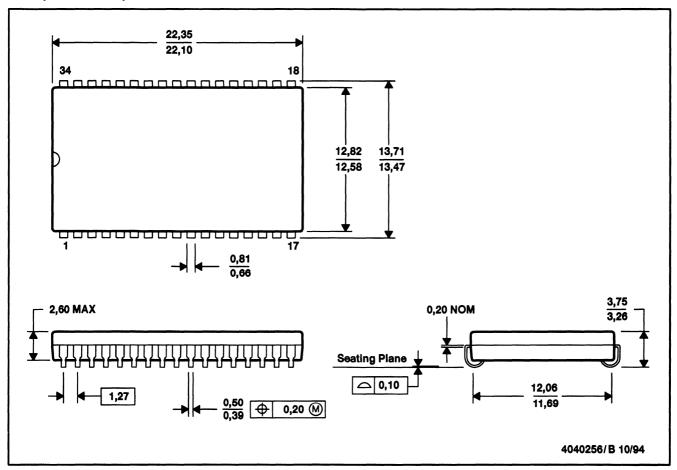
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

DBG (R-PDSO-J34)

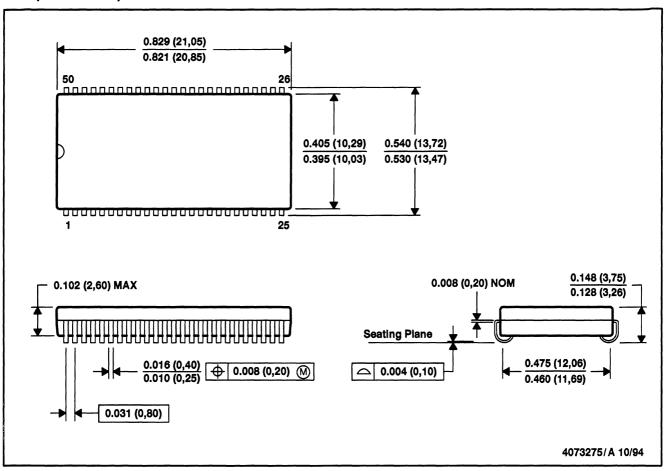
PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- B. This drawing is subject to change without notice.
- C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.28.

DZC (R-PDSO-J50)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

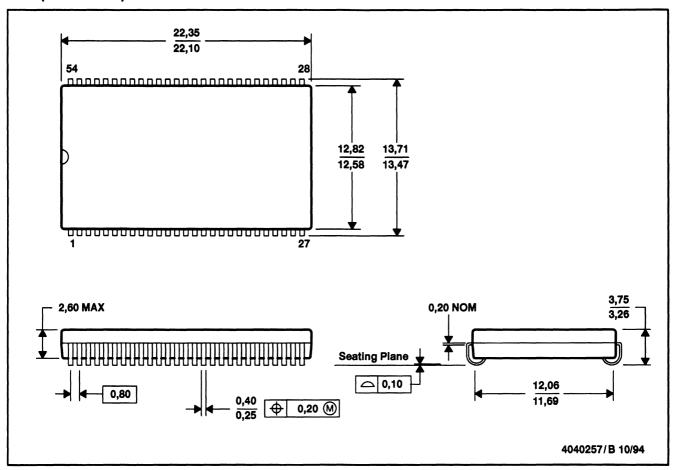
B. This drawing is subject to change without notice.

C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,28).

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DBG (R-PDSO-J54)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



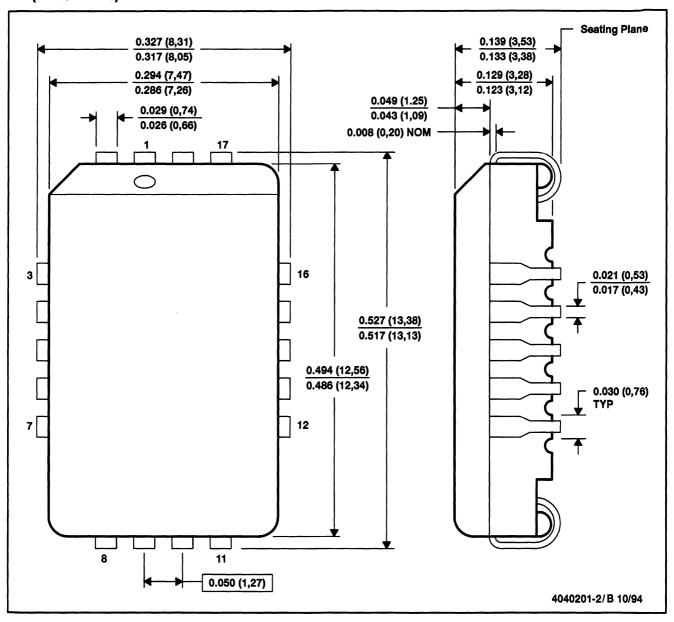
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.28.

FM (R-PQCC-J18)

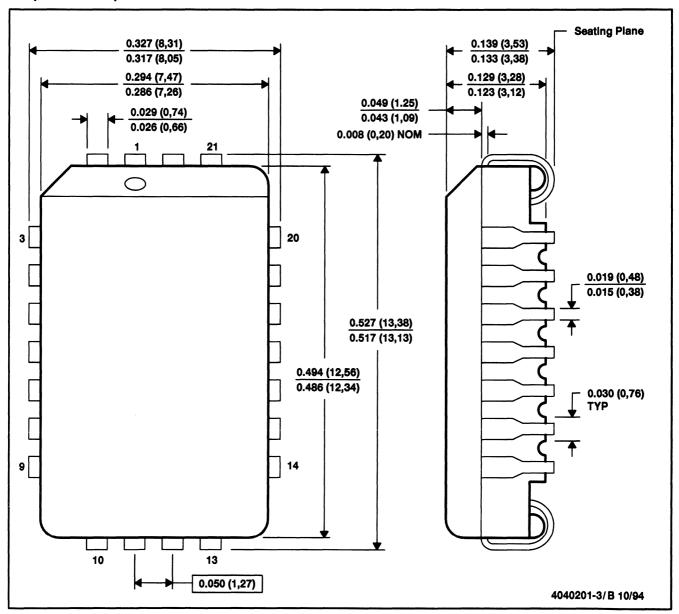
PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

FM (R-PQCC-J22)

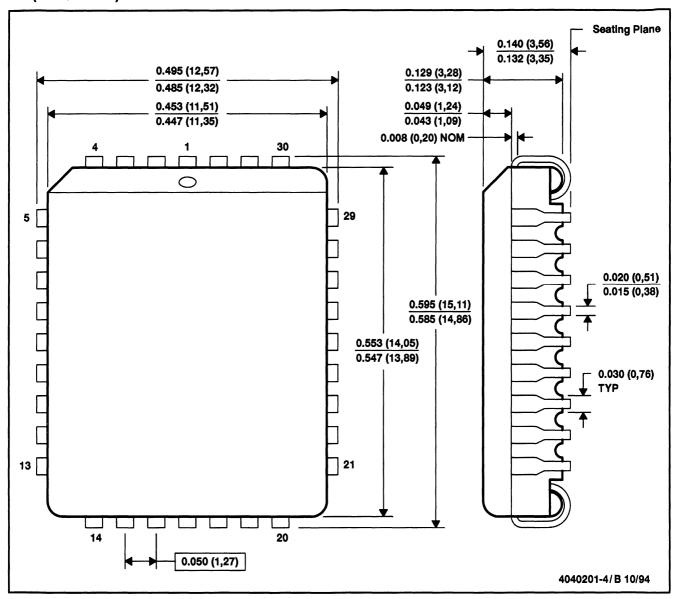
PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

FM (R-PQCC-J32)

PLASTIC J-LEADED CHIP CARRIER

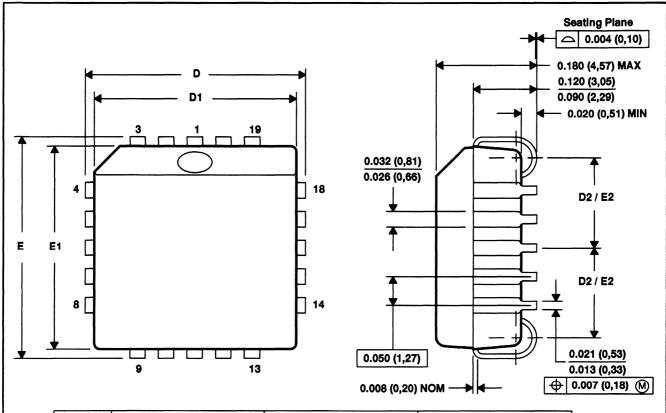


NOTES: A. All linear dimensions are in inches (millimeters).

FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



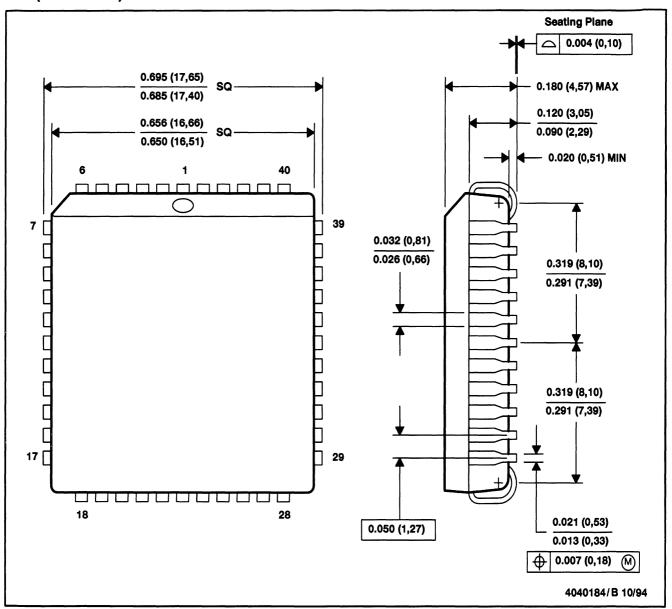
NO. OF PINS **	D/E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-018

FNH (S-PQCC-J44)

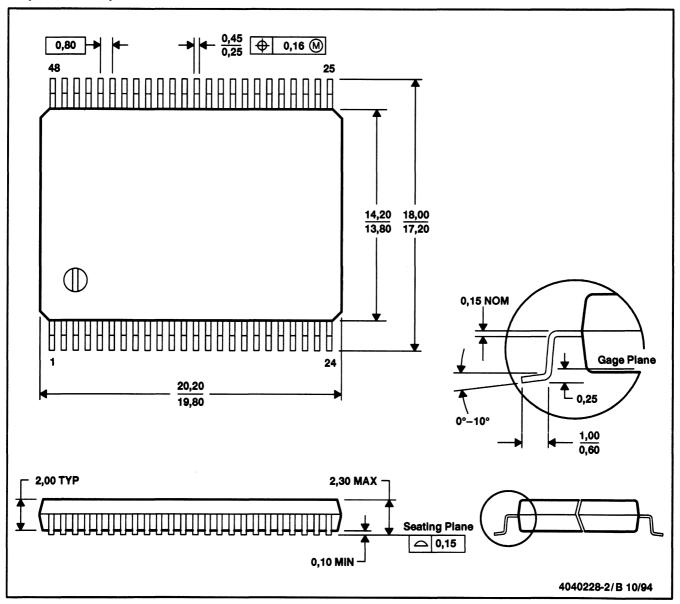
PLASTIC J-LEADED CHIP CARRIER



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-018
- D. Thermally enhanced molded plastic package with leads 19 through 27 connected to the die pad

FT (R-PDFP-G48)

PLASTIC DUAL FLATPACK



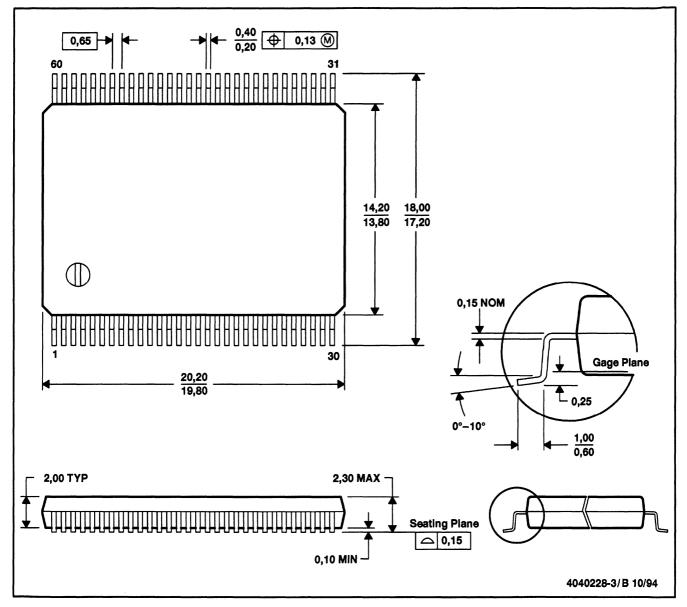
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

FT (R-PDFP-G60)

PLASTIC DUAL FLATPACK

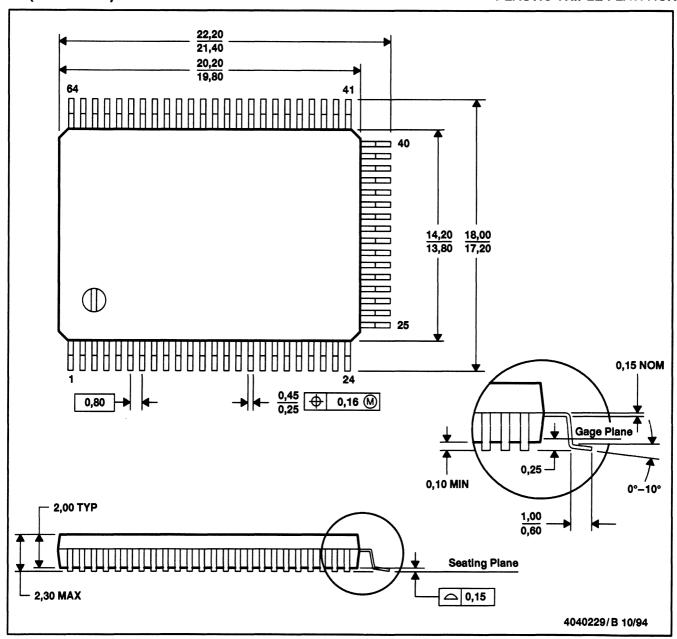


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

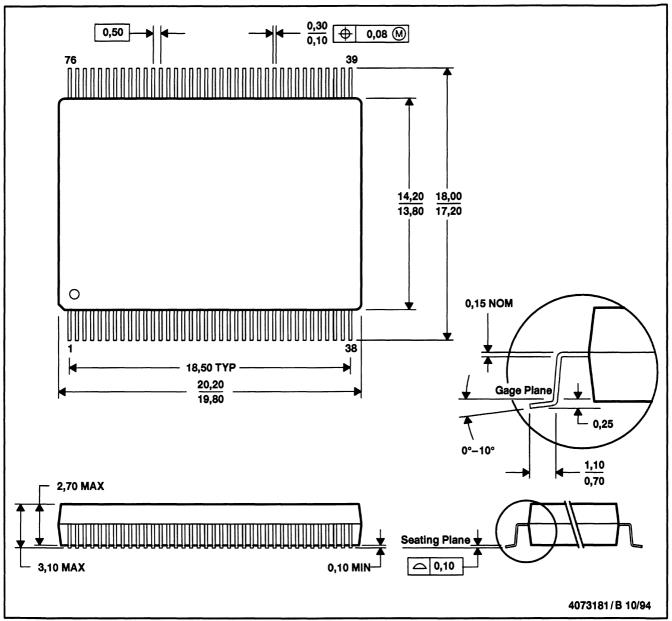
FT (R-PTFP-G64)

PLASTIC TRIPLE FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PDR (R-PDFP-G76)

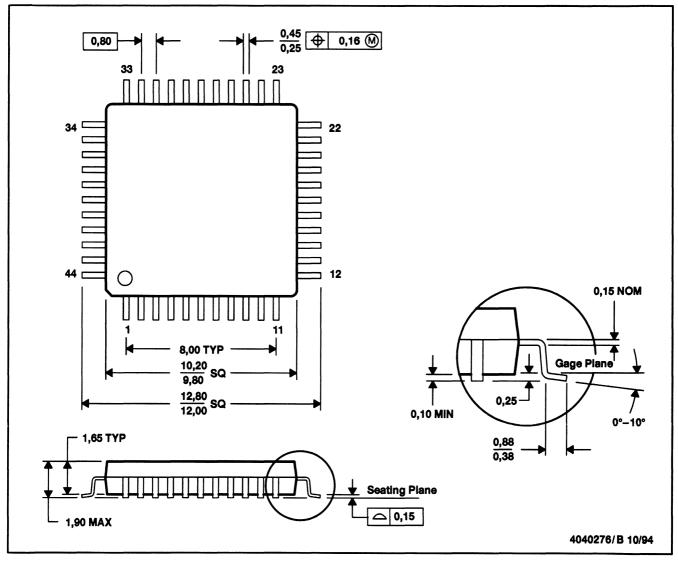


PLASTIC DUAL FLATPACK

- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PAD (S-PQFP-G44)

PLASTIC QUAD FLATPACK



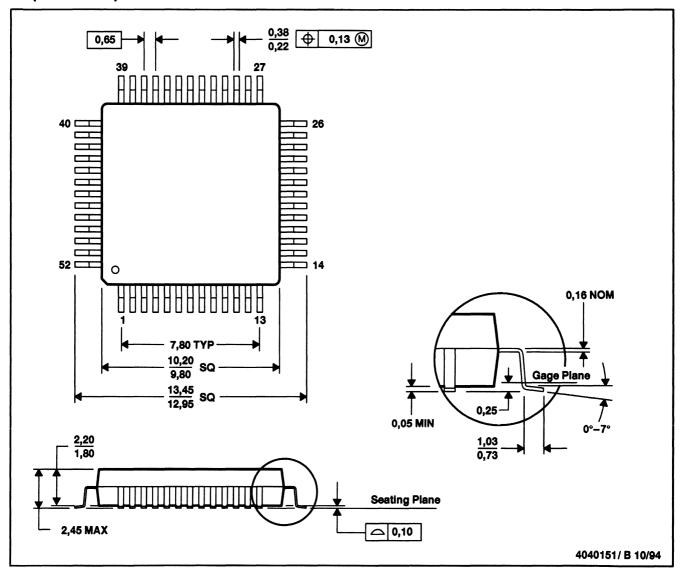
- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PLASTIC QUAD FLATPACK FR (S-PDFP-G44) 0,40 0,80 0,16 M ___ 22 34 🗀 **12** 0,15 NOM 8,00 TYP Gage Plane $\frac{10,20}{9,80}$ SQ 0,25 12,80 12,00 0,10 MIN 0°-10° $\frac{0,88}{0,48}$ 1,75 TYP **Seating Plane** 2,25 MAX **△** 0,10 4040159/B 10/94

NOTES: A. All linear dimensions are in millimeters.

RC (S-PQFP-G52)

PLASTIC QUAD FLATPACK

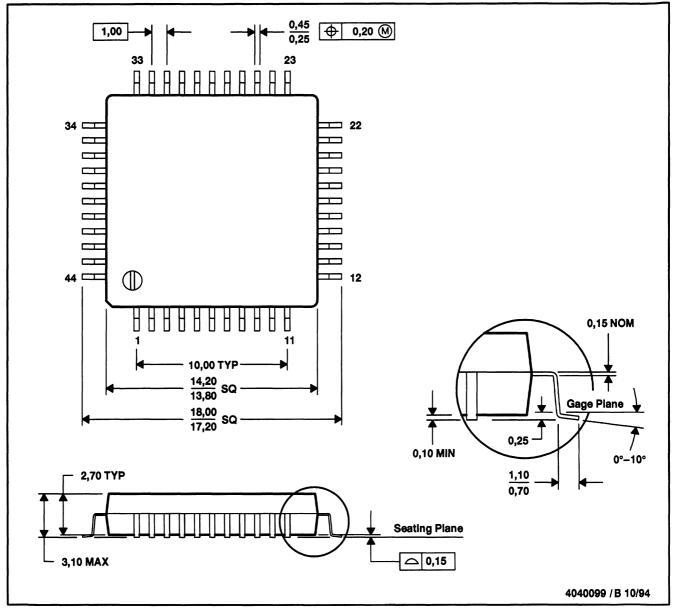


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-022

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PE (S-PQFP-G44)

PLASTIC QUAD FLATPACK



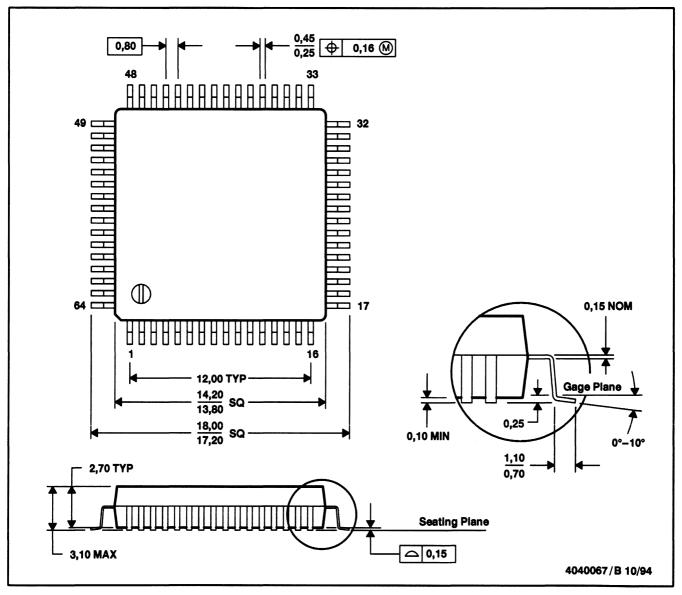
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PF (S-PQFP-G64)

PLASTIC QUAD FLATPACK



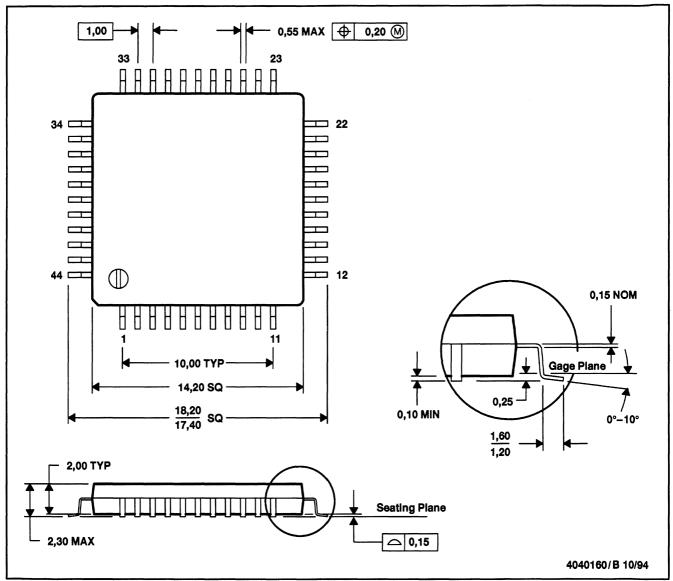
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

FS (S-PQFP-G44)

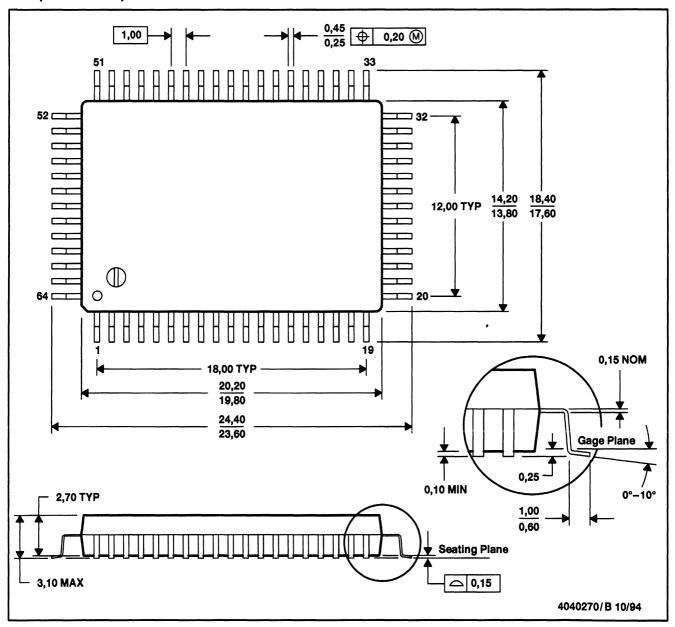
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PAK (R-PQFP-G64)

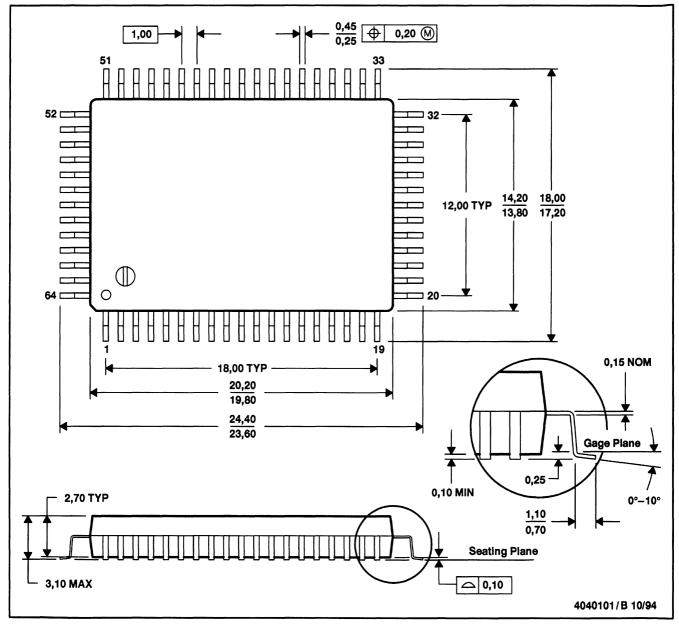
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PG (R-PQFP-G64)

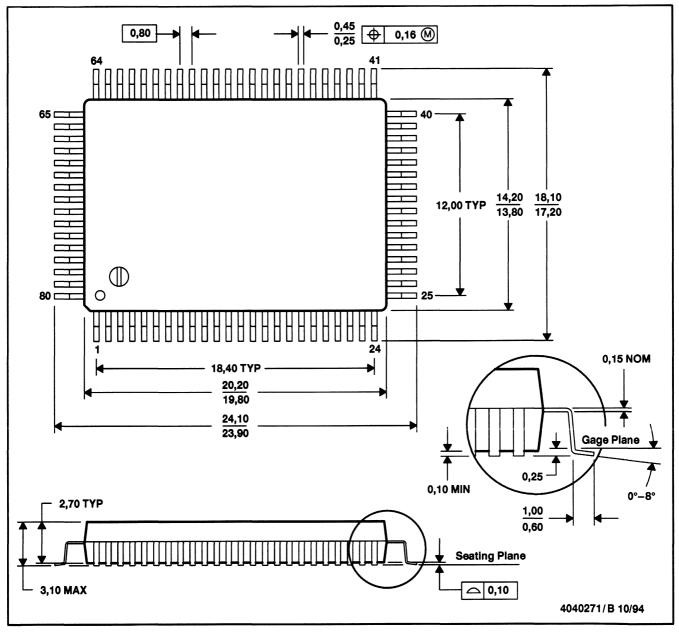
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PAF (R-PQFP-G80)

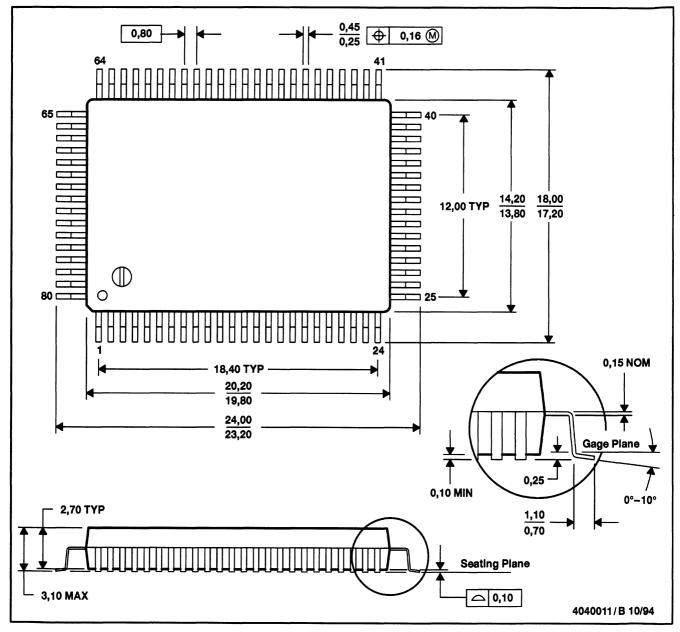
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

PH (R-PQFP-G80)

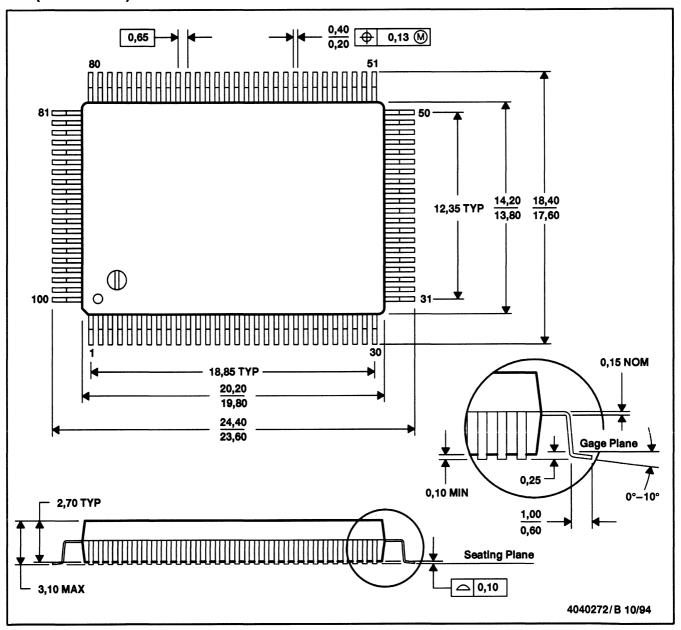
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

PAL (R-PQFP-G100)

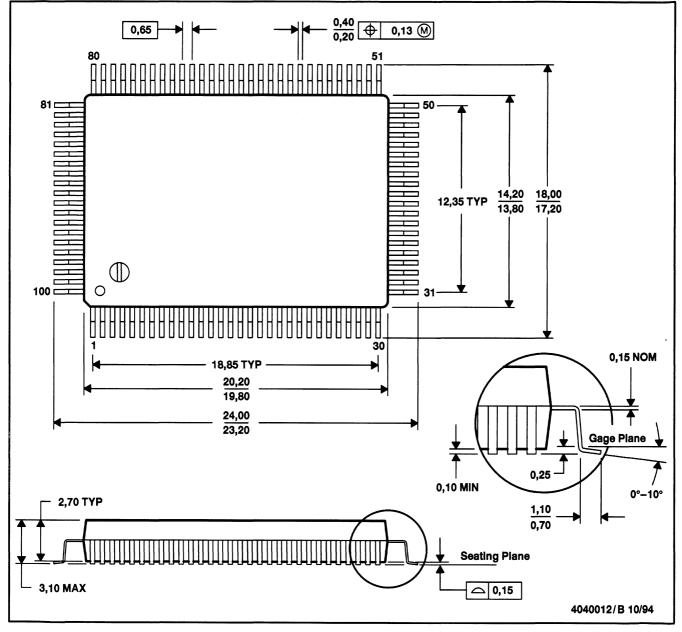
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).

PJ (R-PQFP-G100)

PLASTIC QUAD FLATPACK



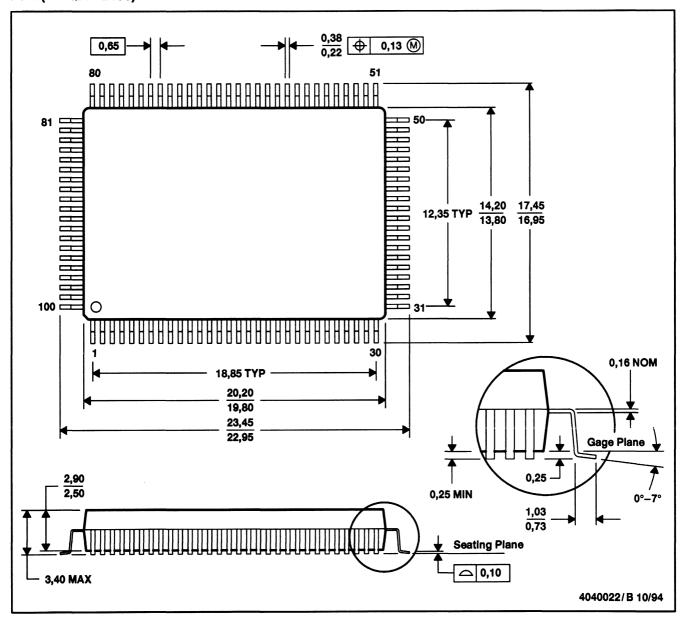
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PJM (R-PQFP-G100)

PLASTIC QUAD FLATPACK



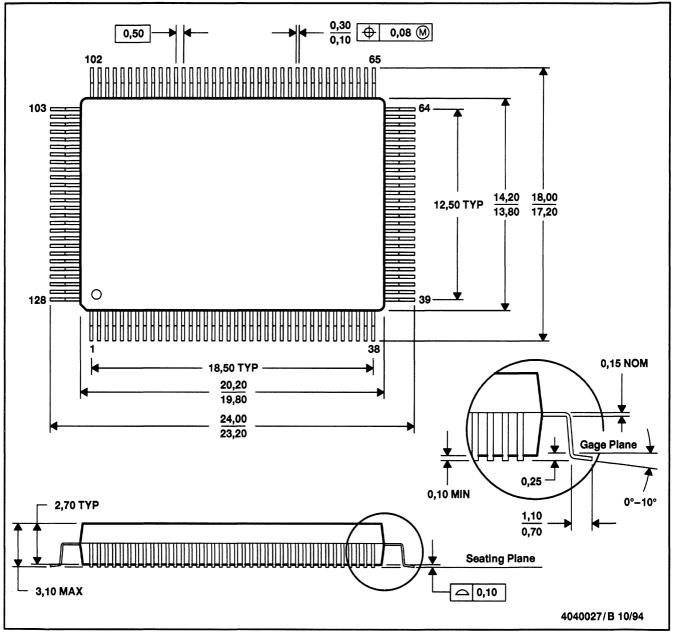
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-022

PR (R-PQFP-G128)

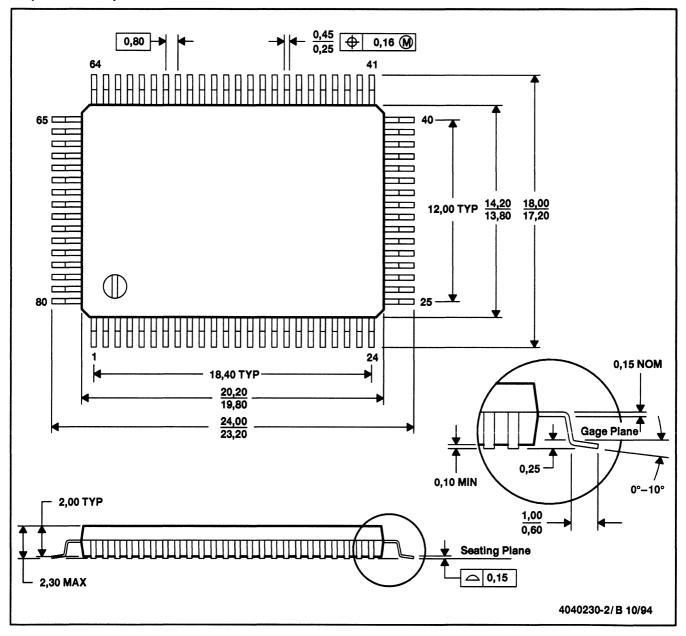
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

FT (R-PQFP-G80)

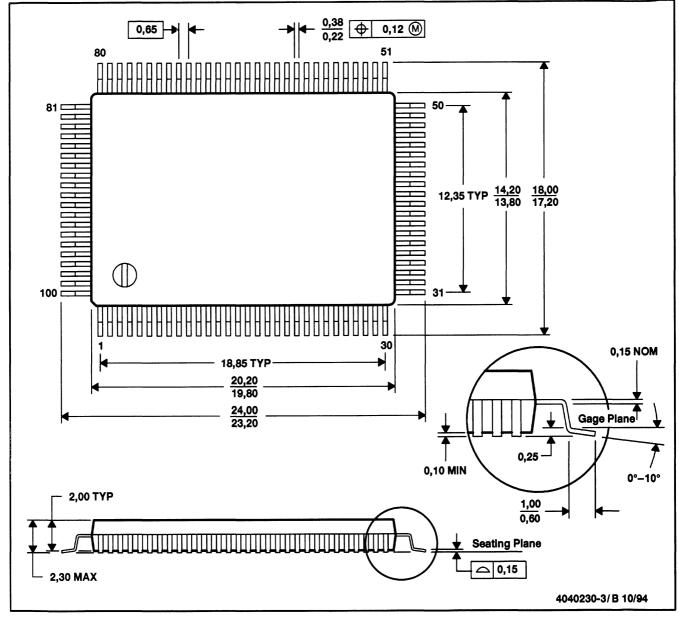
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

FT (R-PQFP-G100)

PLASTIC QUAD FLATPACK



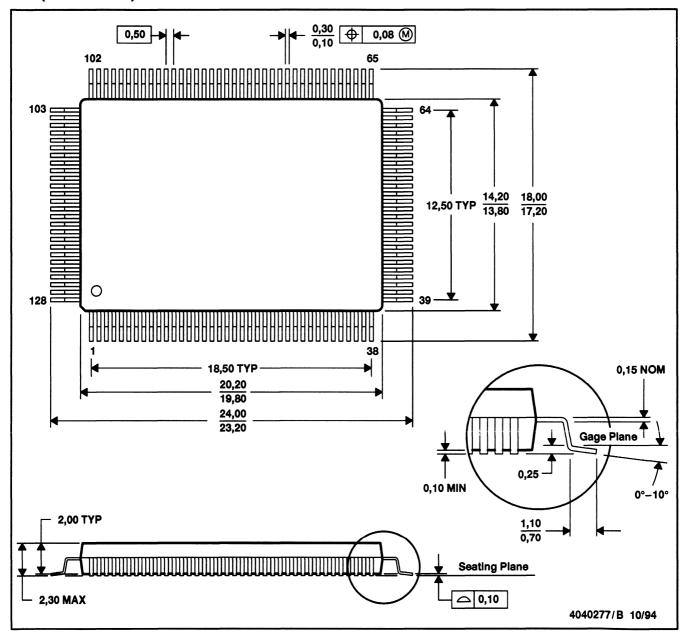
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PGJ (R-PQFP-G128)

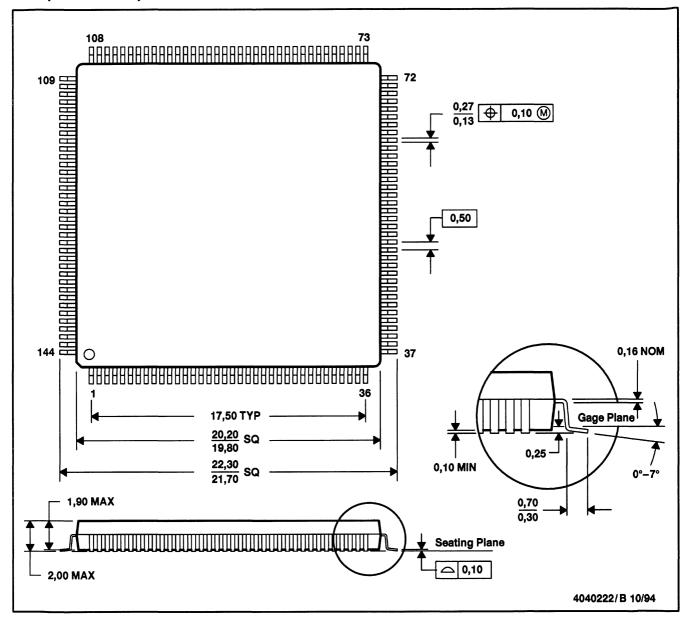
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PGG (S-PQFP-G144)

PLASTIC QUAD FLATPACK



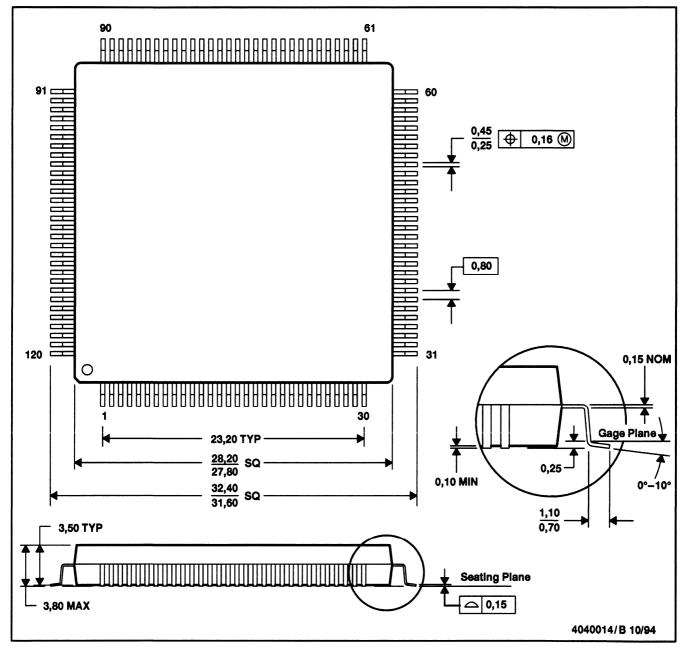
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PB (S-PQFP-G120)

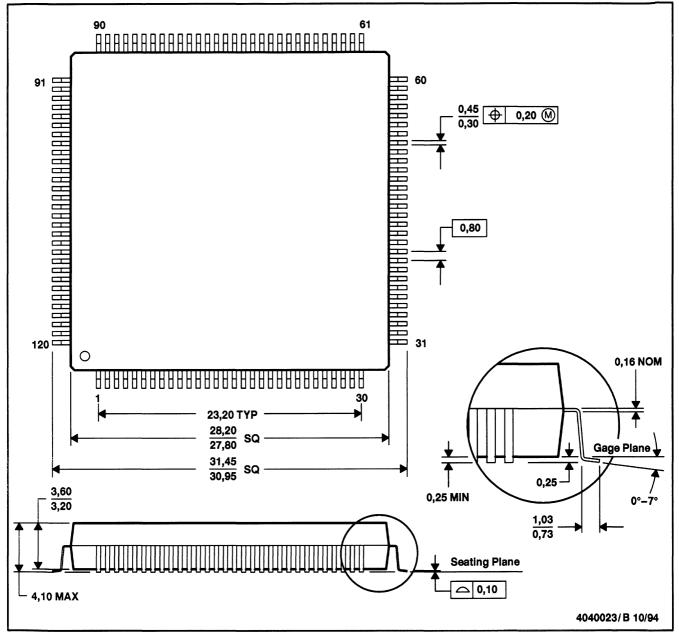
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PBM (S-PQFP-G120)

PLASTIC QUAD FLATPACK

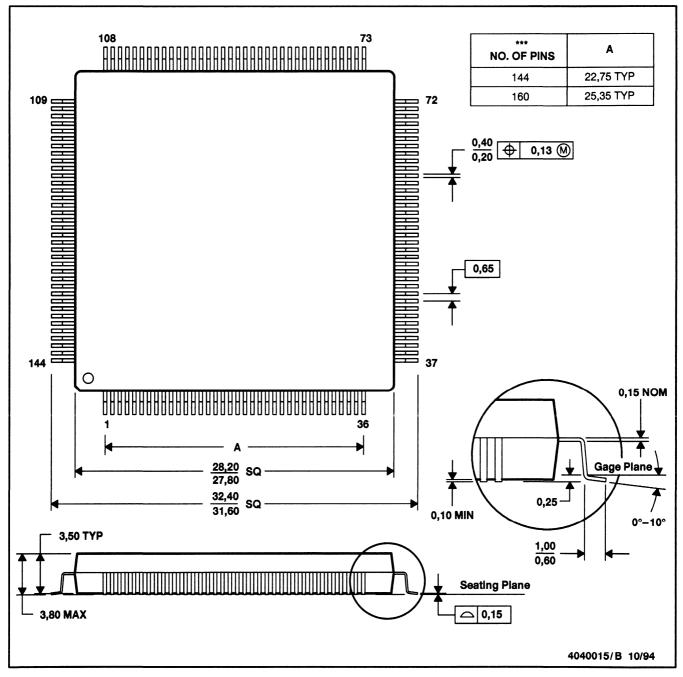


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-022

PC (S-PQFP-G*)**

144 PIN SHOWN

PLASTIC QUAD FLATPACK

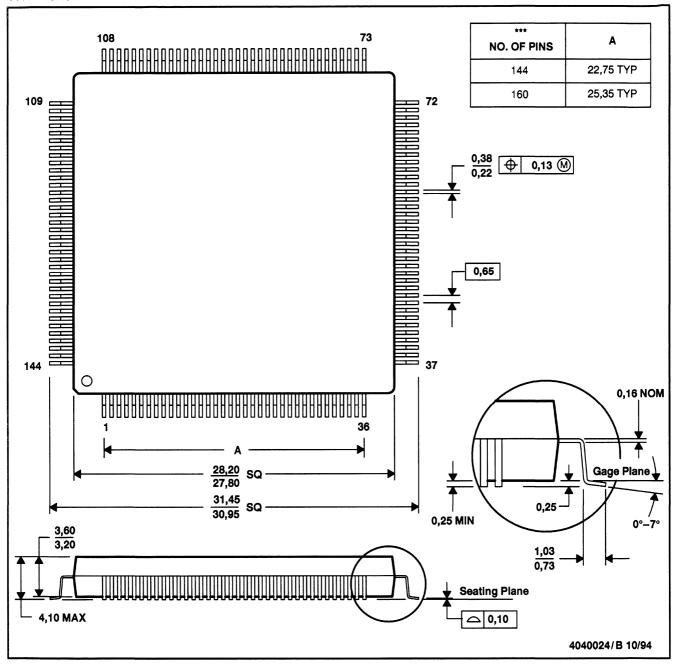


- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PCM (S-PQFP-G***)

PLASTIC QUAD FLATPACK

144 PIN SHOWN

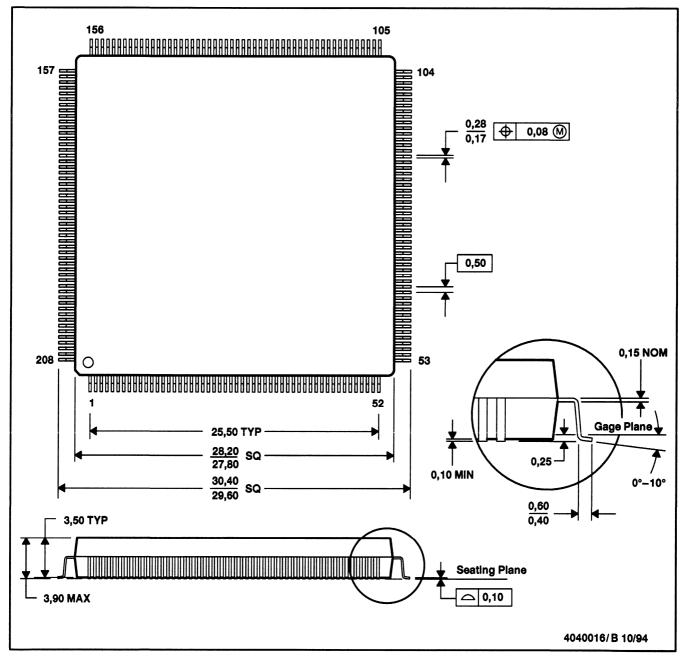


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-022
- D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.



PP (S-PQFP-G208)

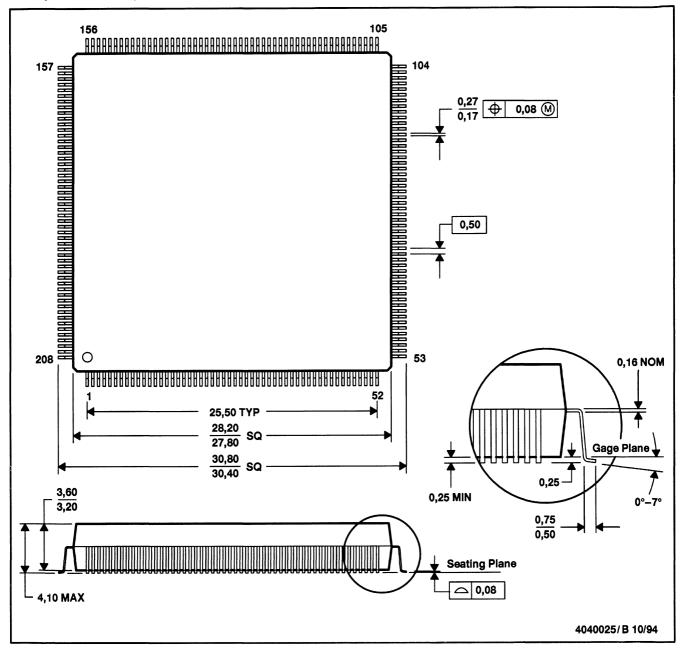
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PPM (S-PQFP-G208)

PLASTIC QUAD FLATPACK



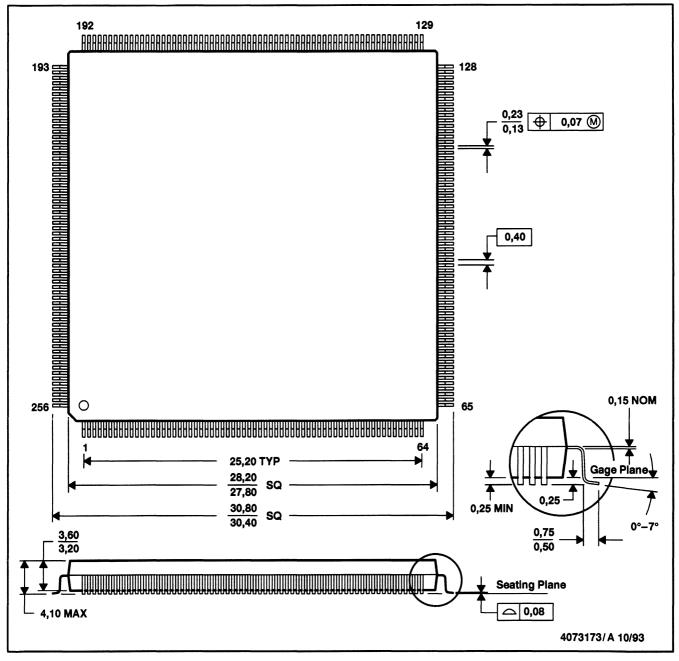
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO-143

PGH (S-PQFP-G256)

PLASTIC QUAD FLATPACK

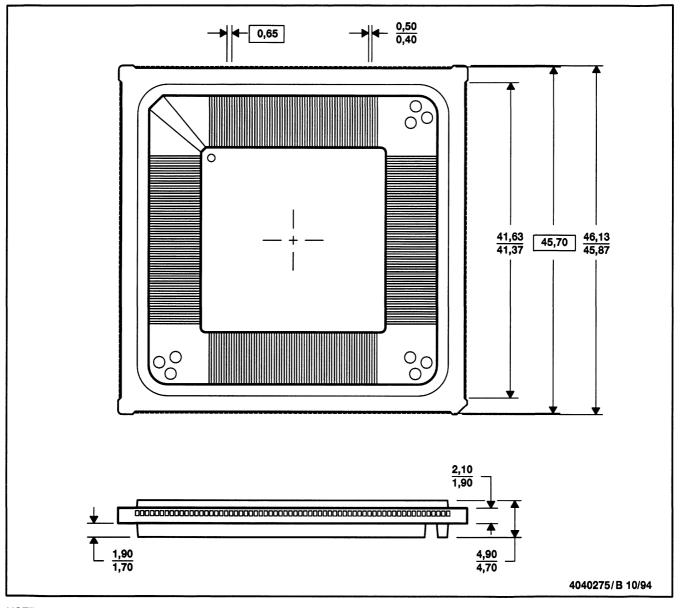


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-143

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PAB (S-PQFP-F136)

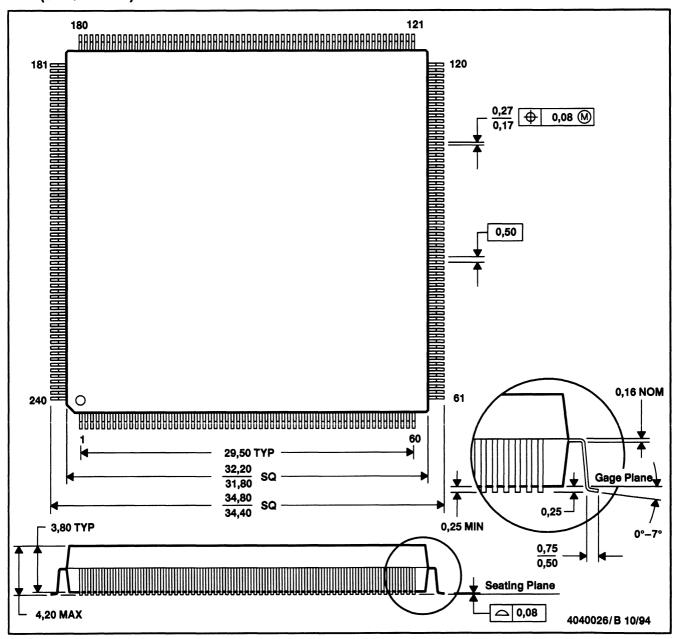
PLASTIC QUAD FLATPACK (CARRIER RING)



NOTES: A. All linear dimensions are in millimeters.

PGC (S-PQFP-G240)

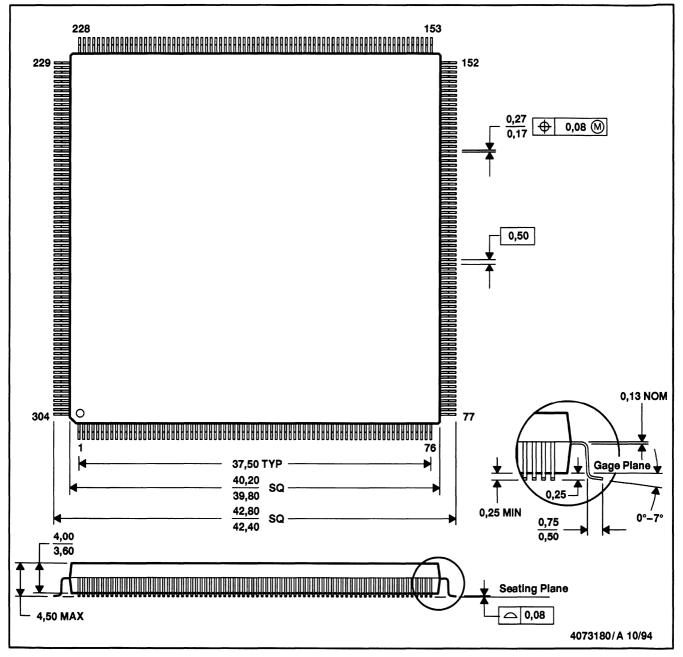
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

PDN (S-PQFP-G304)

PLASTIC QUAD FLATPACK (DIE-DOWN)

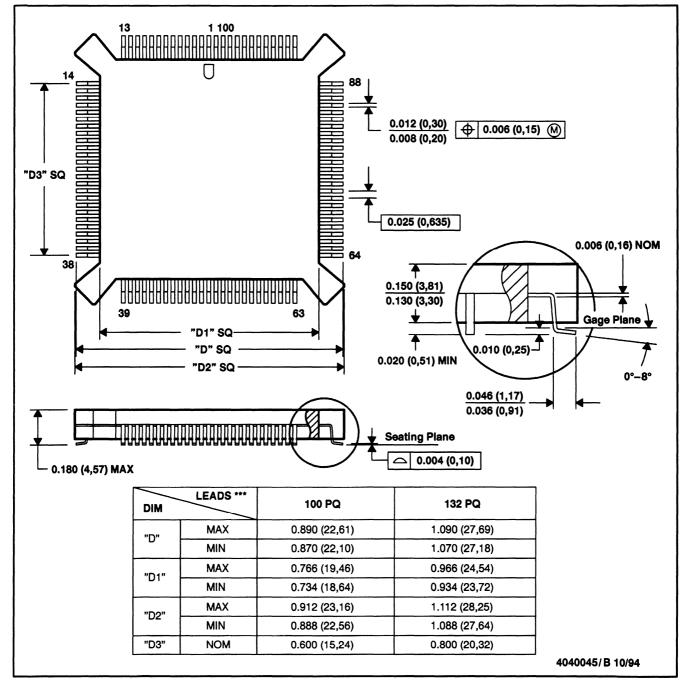


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-143

PQ (S-PQFP-G***)

PLASTIC QUAD FLATPACK

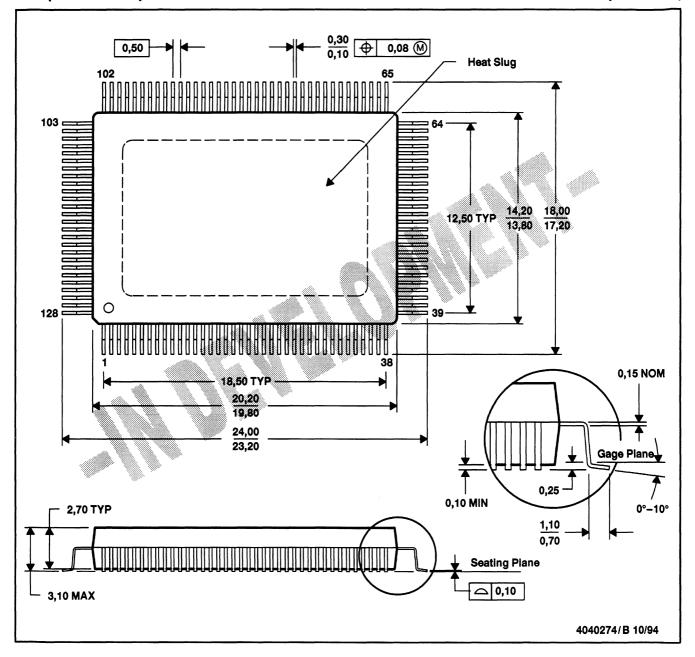
100 LEAD SHOWN



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-069

PAC (R-PQFP-G128)

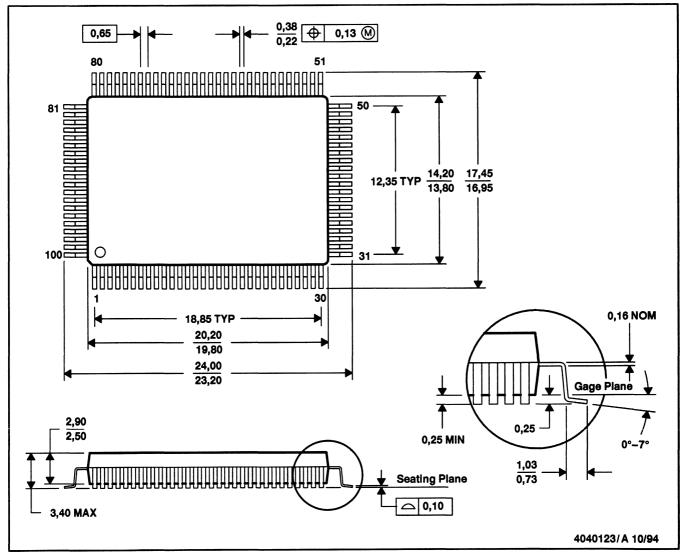
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package (HSL) exposed on package bottom
- D. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

PJE (R-PQFP-G100)

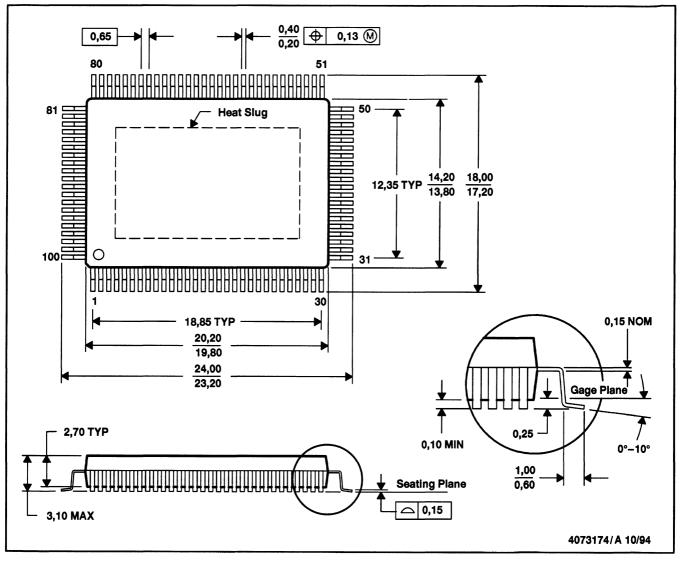
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MS-022

PJG (R-PQFP-G100)

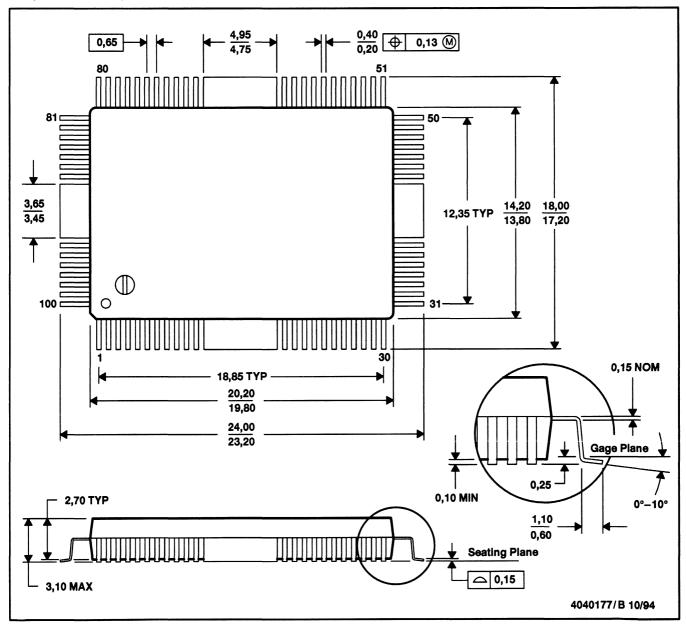
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.
- D. Thermally enhanced molded plastic package with a heat slug (HSL) exposed on package bottom

VH (S-PQFP-G100)

PLASTIC QUAD FLATPACK



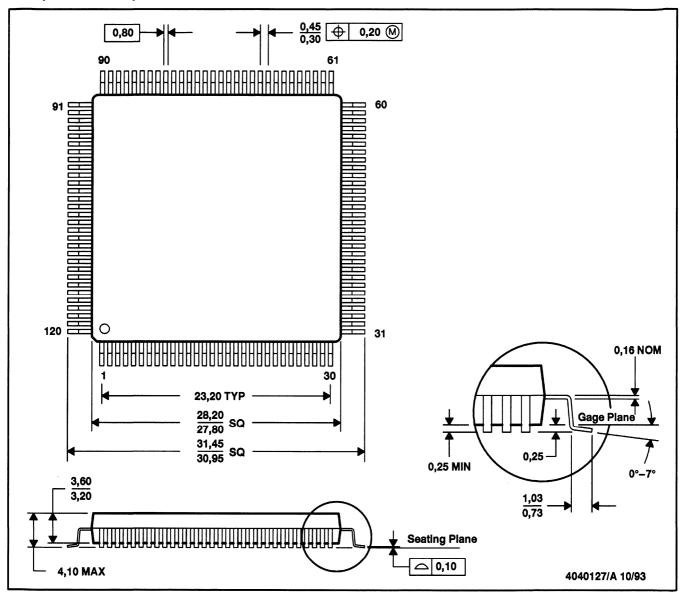
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Thermal enhancement with fins attached to faced heat spreader

PBE (S-PQFP-G120)

PLASTIC QUAD FLATPACK

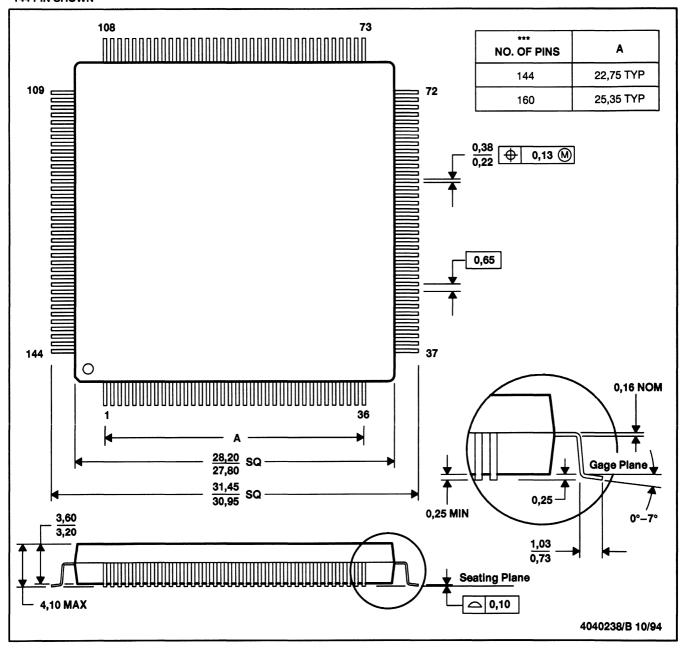


- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MS-022

PCD (S-PQFP-G***)

PLASTIC QUAD FLATPACK (DIE-DOWN)

144 PIN SHOWN

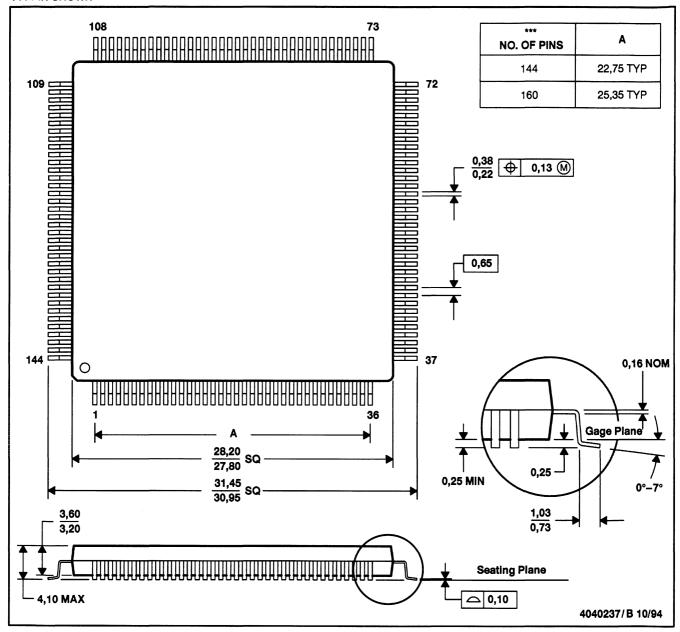


- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MS-022
- E. The 144 PCD is identical to the 160 PCD except that four leads per corner are removed.

PCE (S-PQFP-G***)

PLASTIC QUAD FLATPACK

144 PIN SHOWN

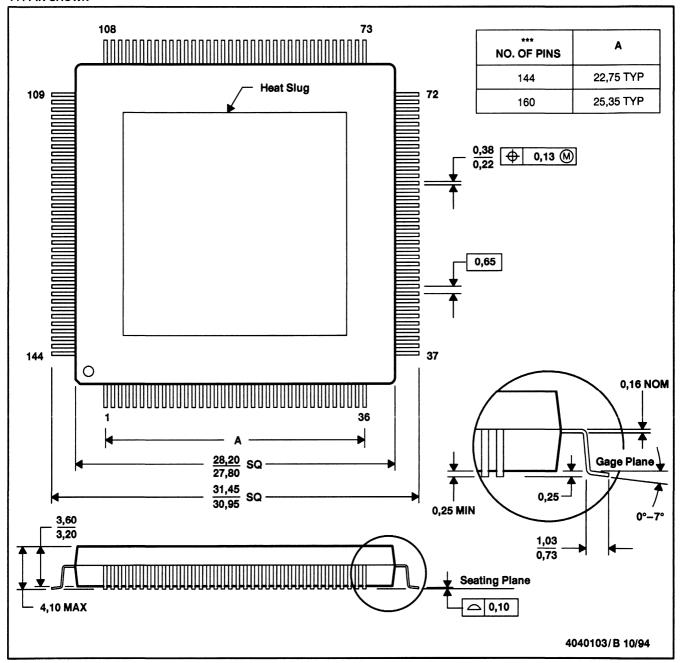


- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MS-022
- E. The 144 PCE is identical to the 160 PCE except that four leads per corner are removed.

PCY (S-PQFP-G***)

PLASTIC QUAD FLATPACK

144 PIN SHOWN

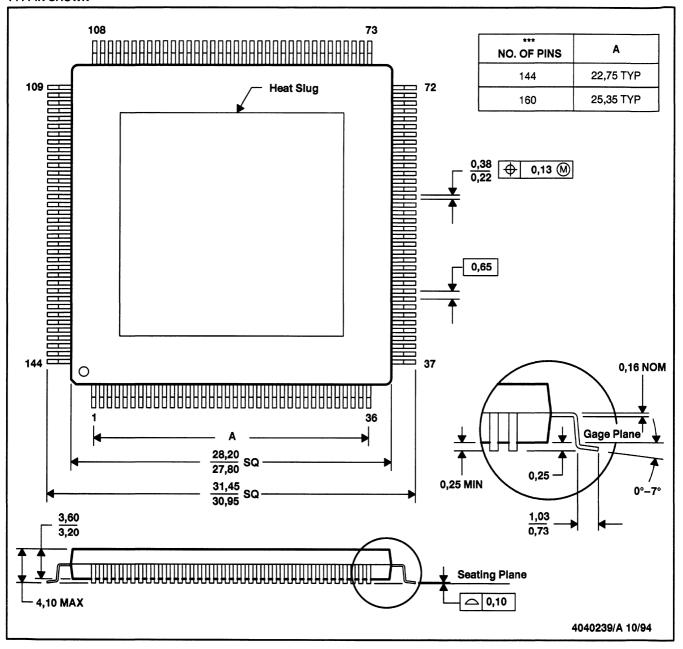


- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)
- D. Falls within JEDEC MS-022
- E. The 144 PCY is identical to the 160 PCY except that four leads per corner are removed.

PCZ (S-PQFP-G**)

PLASTIC QUAD FLATPACK (DIE-DOWN)

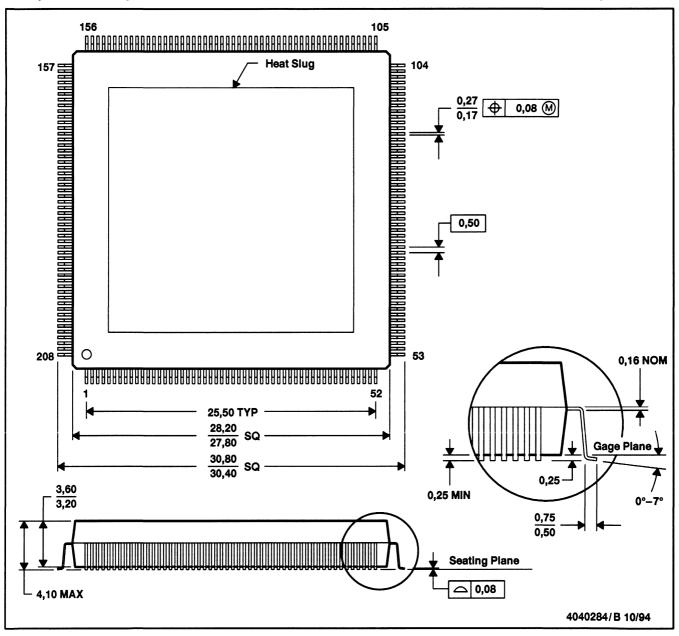
144 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)
- D. Falls within JEDEC MS-022
- E. The 144 PCZ is identical to the 160 PCZ except that four leads per corner are removed.

PPB (S-PQFP-G208)

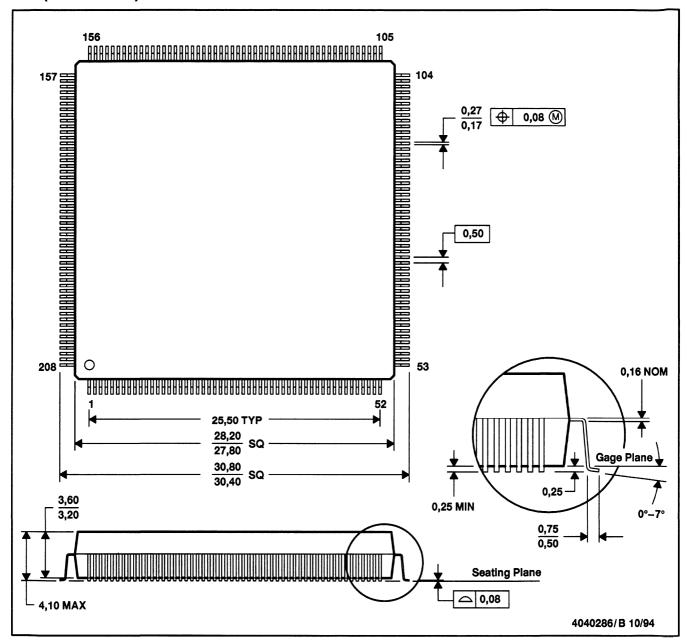
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)
- D. Falls within JEDEC MO-143

PPE (S-PQFP-G208)

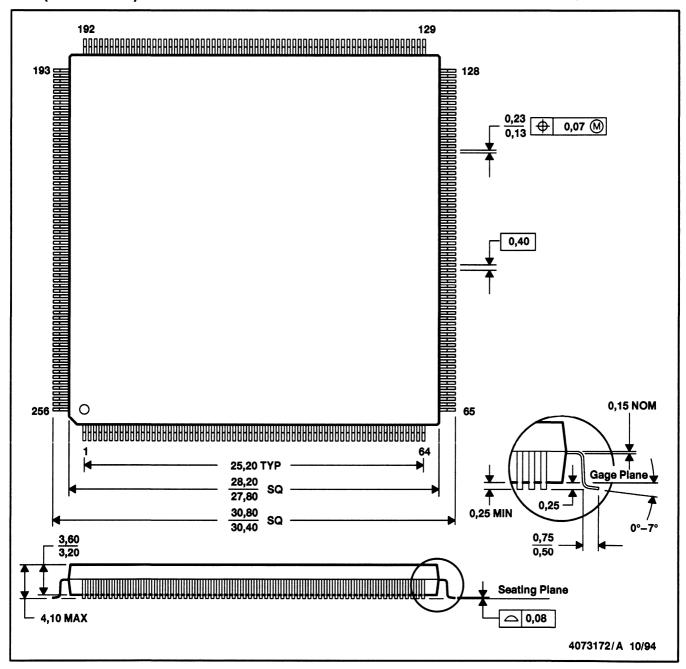
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MO-143

PGK (S-PQFP-G256)

PLASTIC QUAD FLATPACK

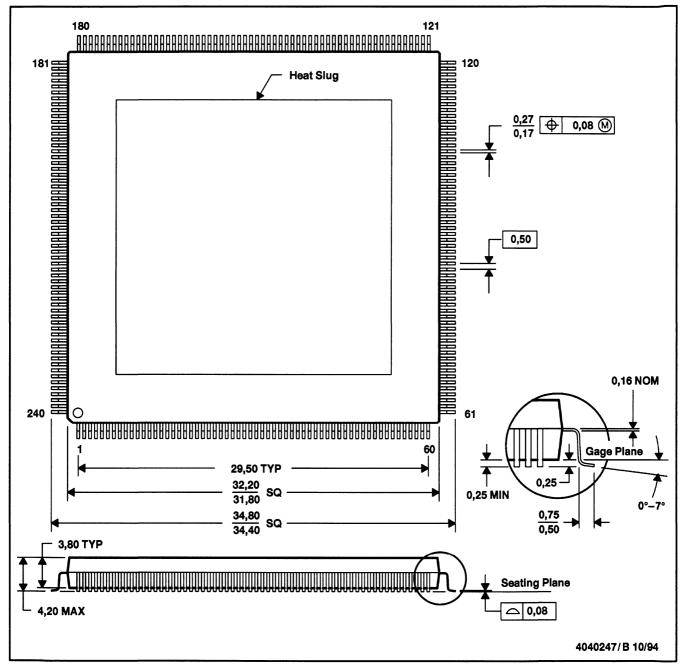


- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)
- D. Falls within JEDEC MO-143



PGV (S-PQFP-G240)

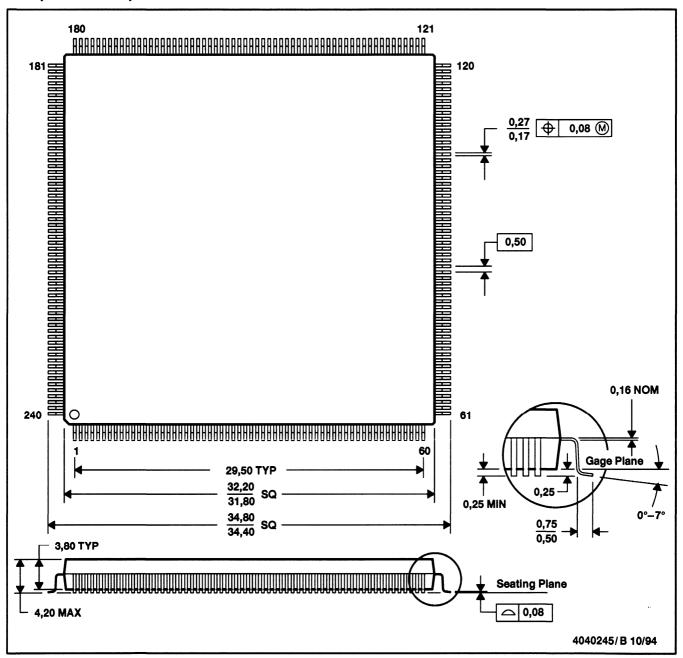
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)

PGY (S-PQFP-G240)

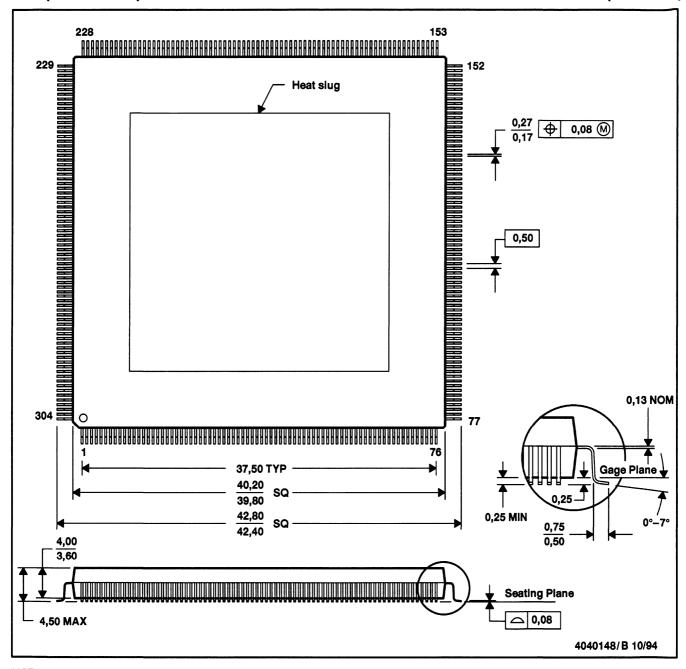
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat spreader (HSP)

PDB (S-PQFP-G304)

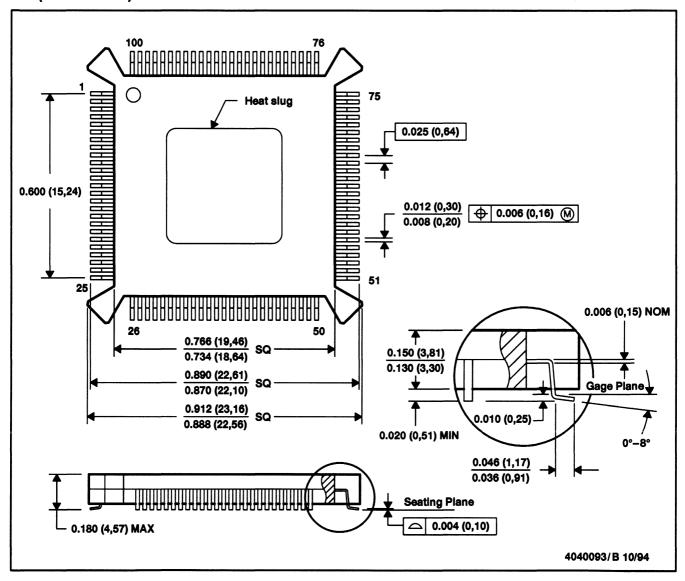
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)
- D. Falls within JEDEC MO-143

PJF (S-PQFP-G100)

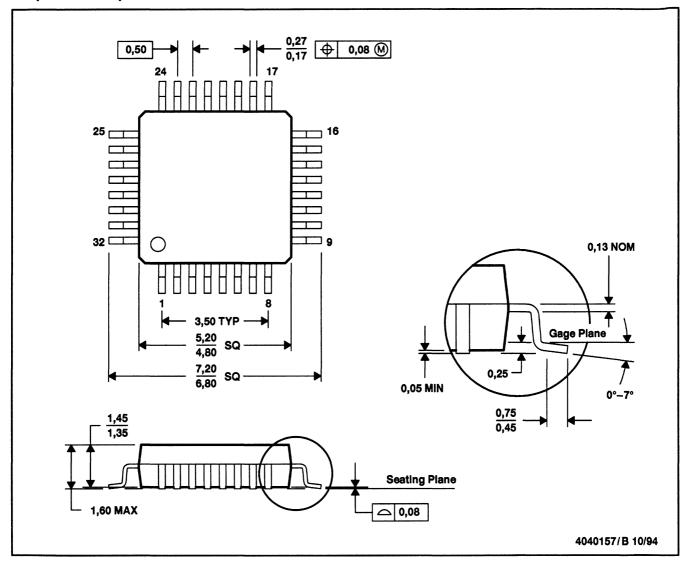
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-143
- D. Thermally enhanced molded plastic package with a heat slug (HSL)

PU (S-PQFP-G32)

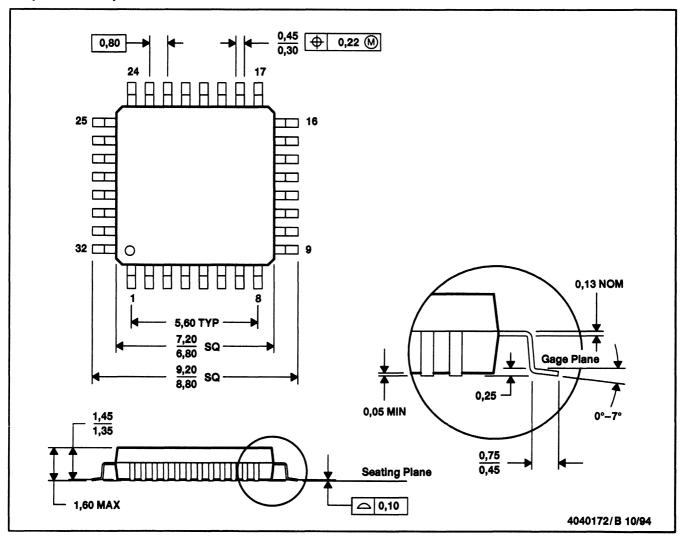
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

VF (S-PQFP-G32)

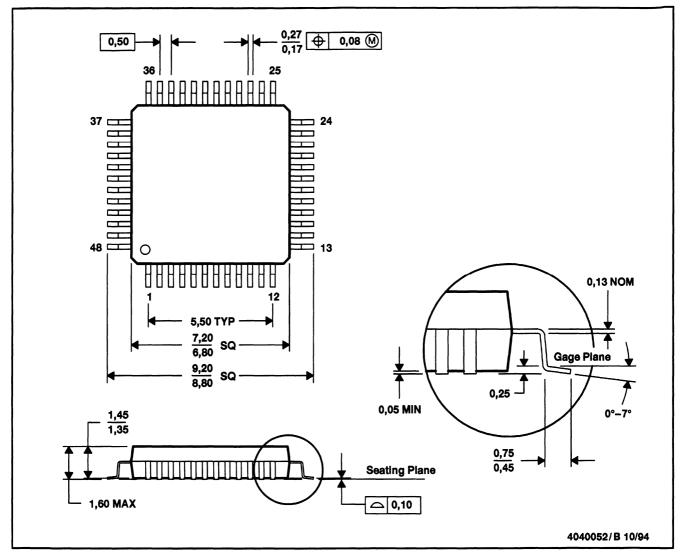
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PT (S-PQFP-G48)

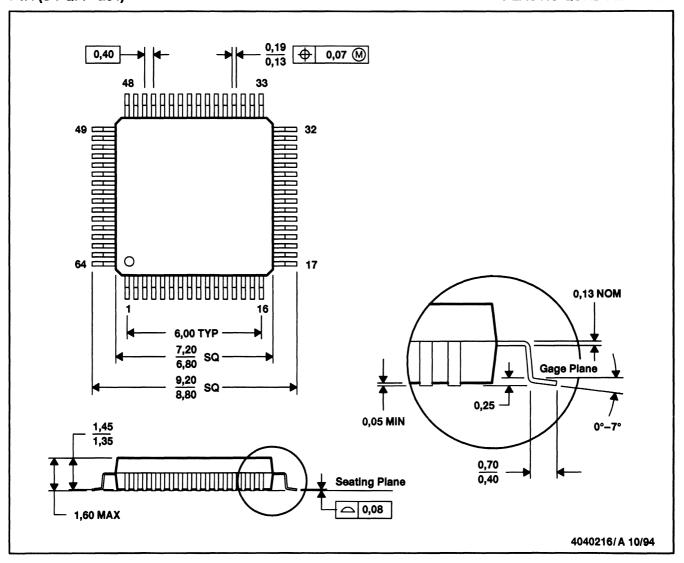
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136
- D. Also may be a thermally enhanced plastic package with leads conected to the die pads

PTA (S-PQFP-G64)

PLASTIC QUAD FLATPACK

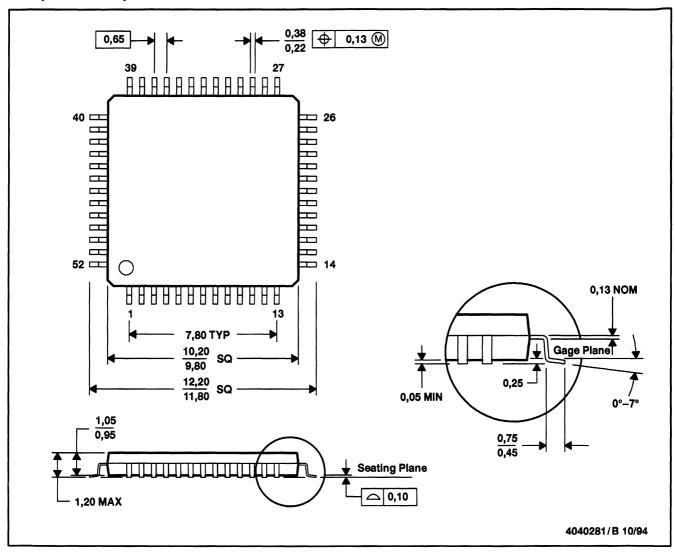


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PAH (S-PQFP-G52)

PLASTIC QUAD FLATPACK

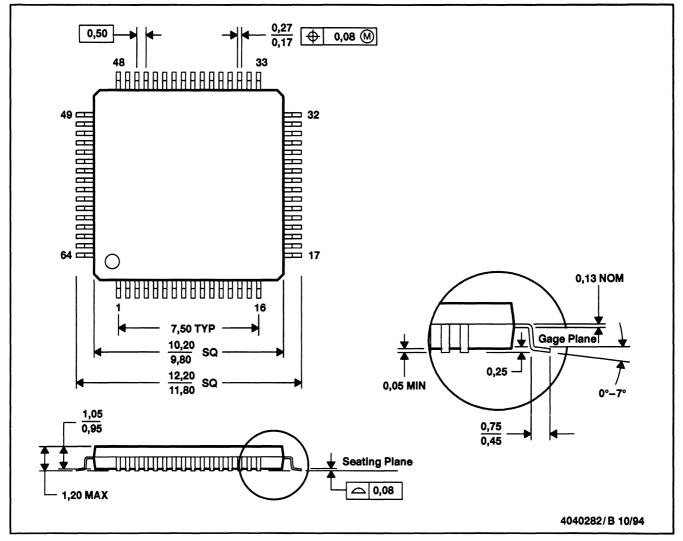


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK

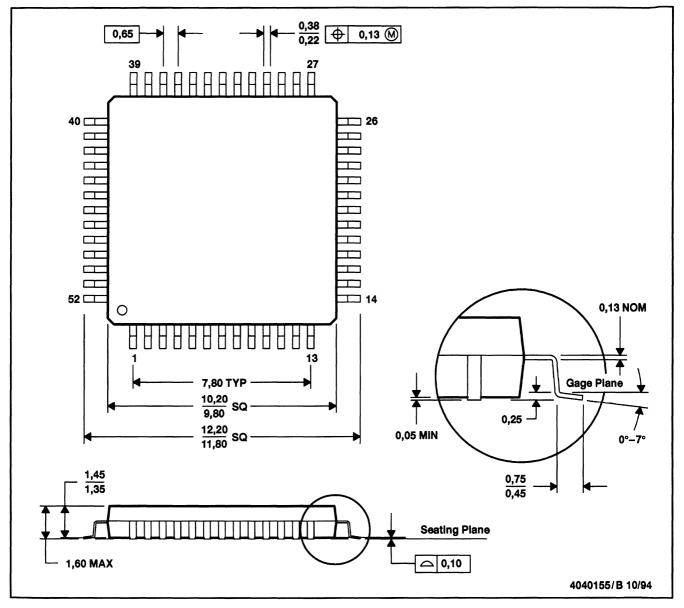


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PBG (S-PQFP-G52)

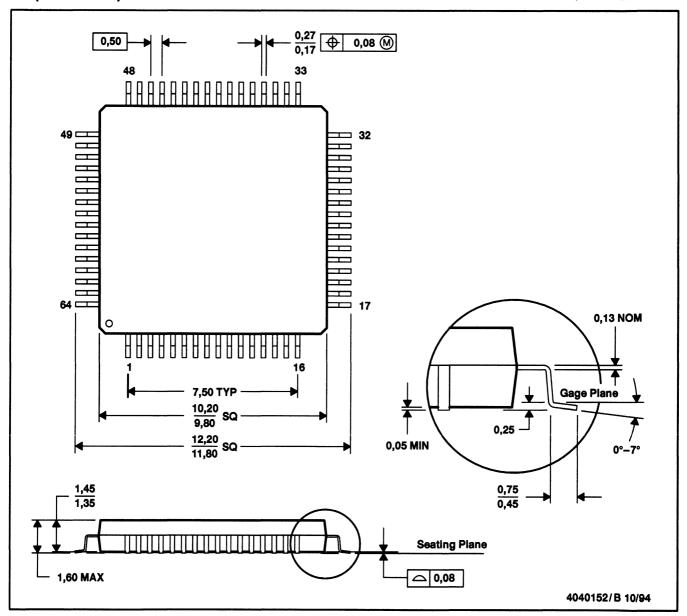
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK

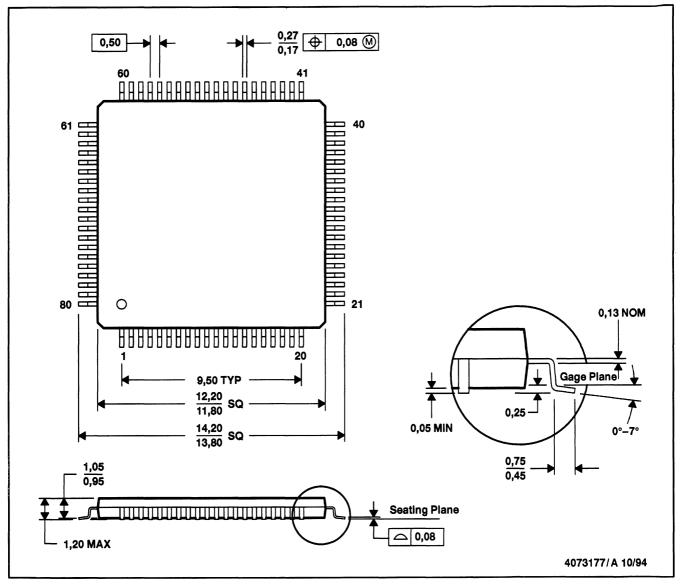


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PFC (S-PQFP-G80)

PLASTIC QUAD FLATPACK

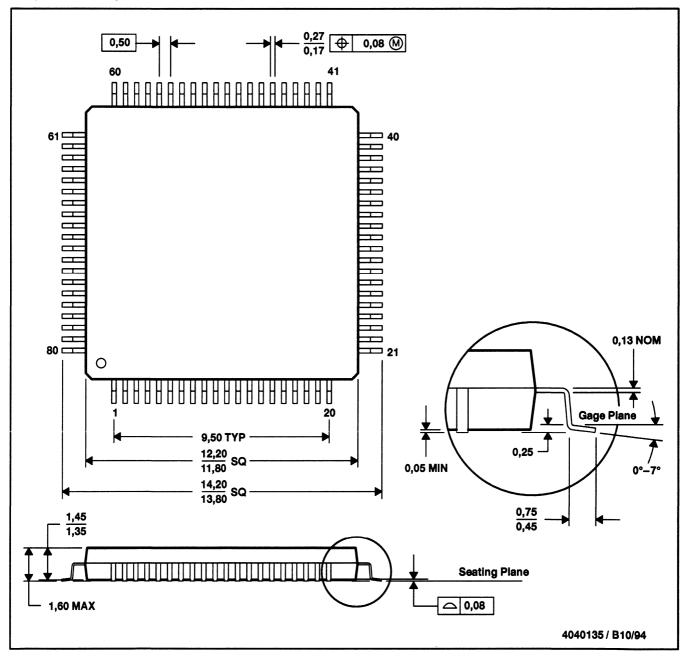


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PN (S-PQFP-G80)

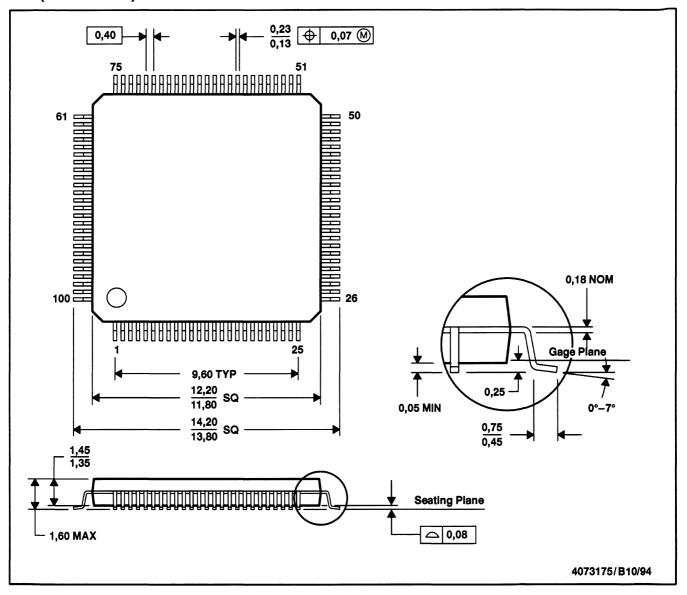
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PFA (S-PQFP-G100)

PLASTIC QUAD FLATPACK

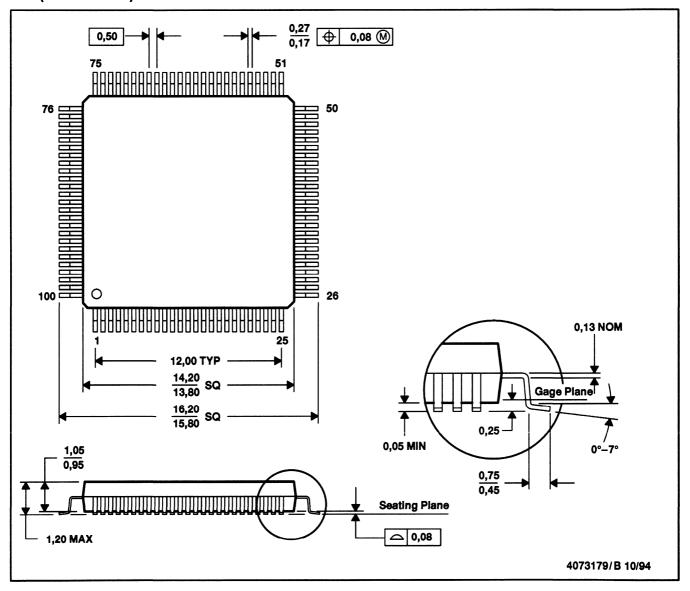


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PZT (S-PQFP-G100)

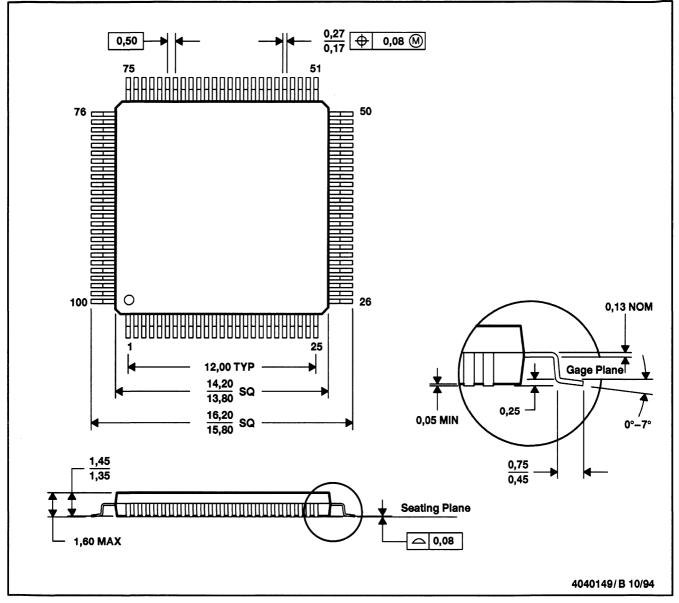
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK

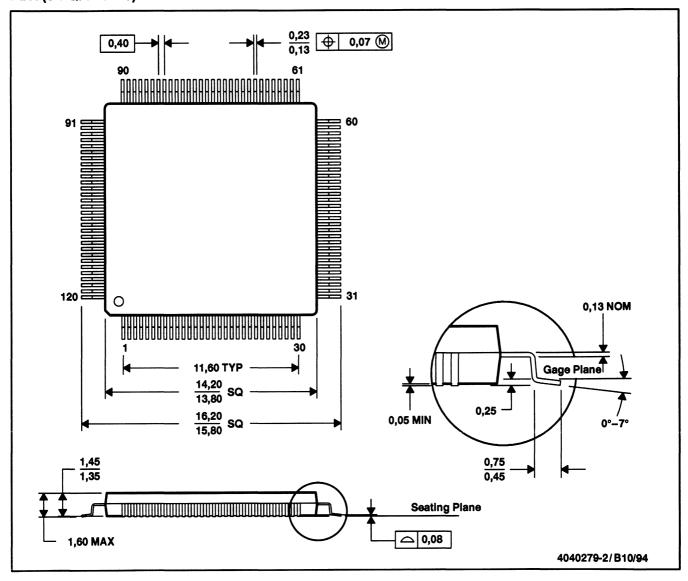


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PBK (S-PQFP-G120)

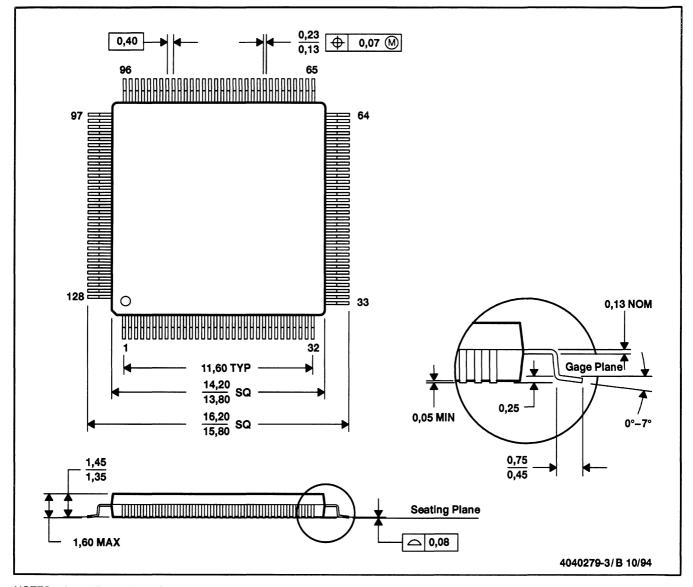
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-136

PBK (S-PQFP-G128)

PLASTIC QUAD FLATPACK

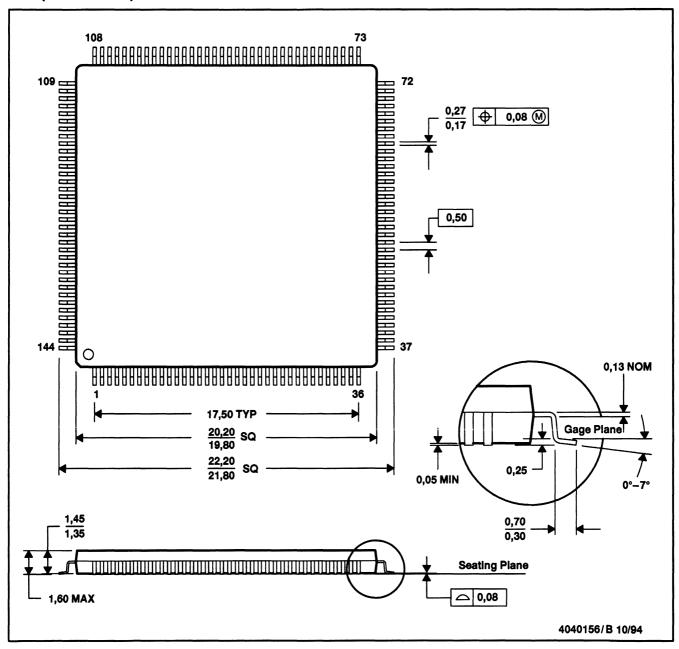


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PGD (S-PQFP-G144)

PLASTIC QUAD FLATPACK

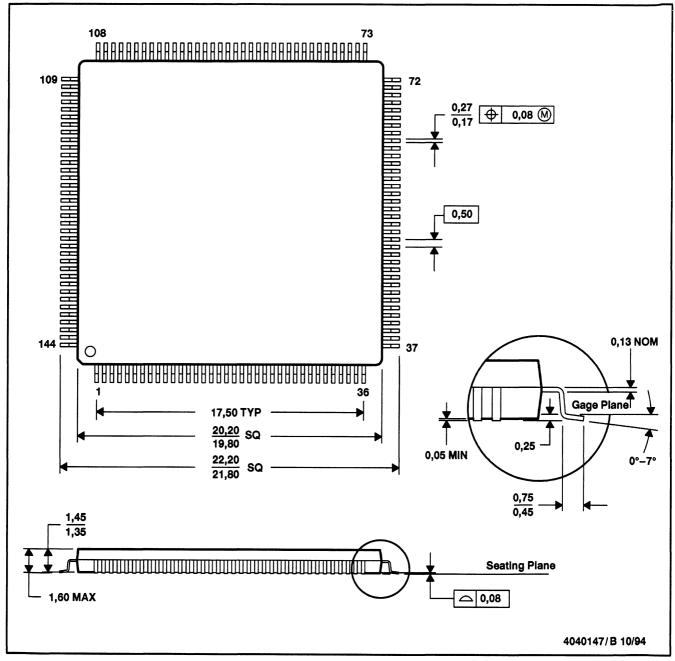


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



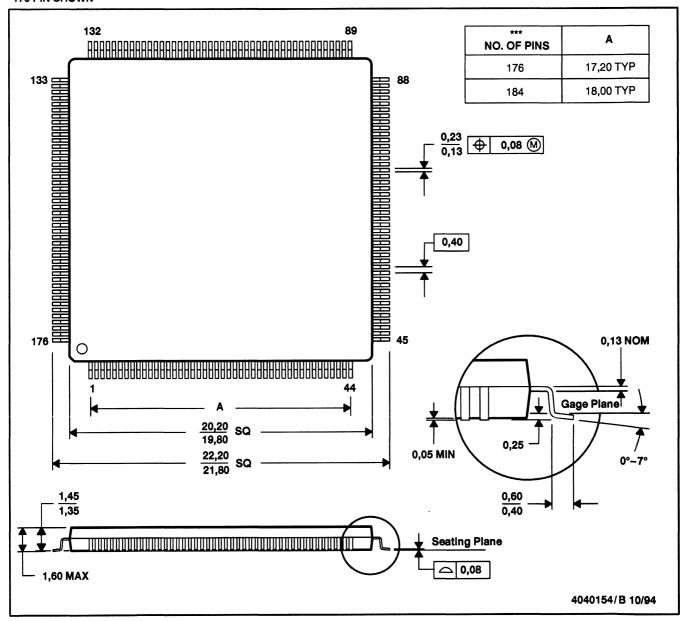
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PBL (S-PQFP-G***)

PLASTIC QUAD FLATPACK

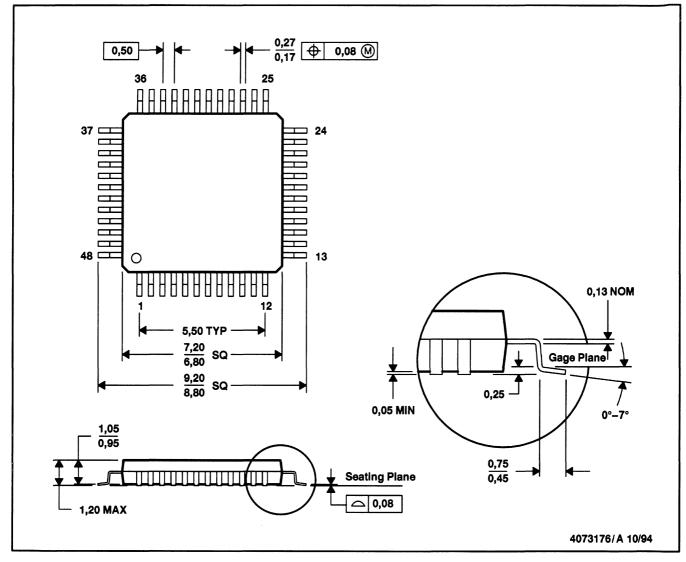
176 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK

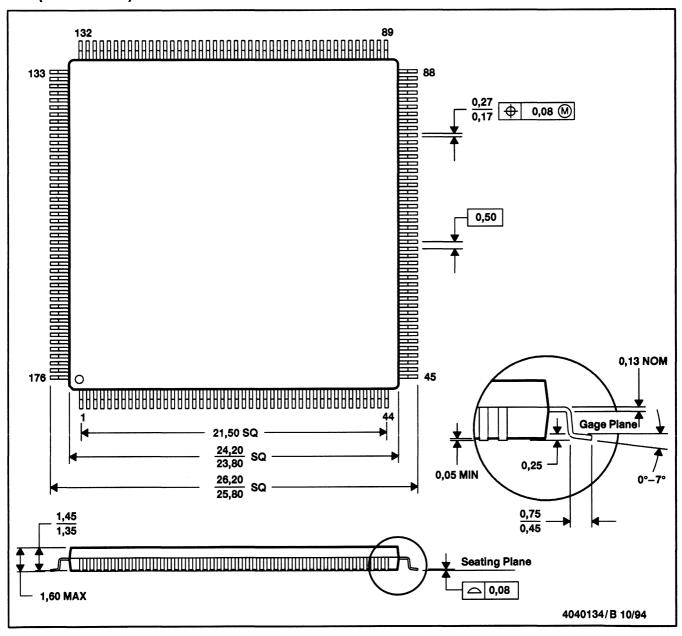


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PGF (S-PQFP-G176)

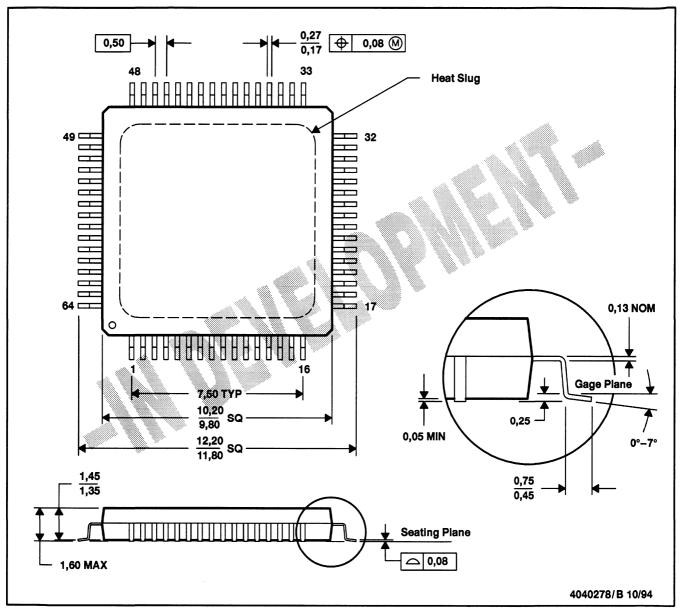
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PAJ (S-PQFP-G64)

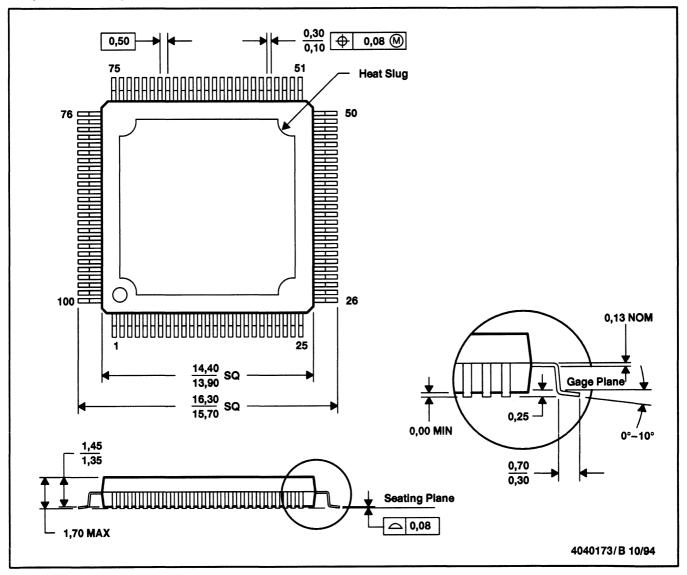
PLASTIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. Thermally enhanced plastic package with a heat slug (HSL) exposed on package bottom
- D. Falls within JEDEC MO-136

VG (S-PQFP-G100)

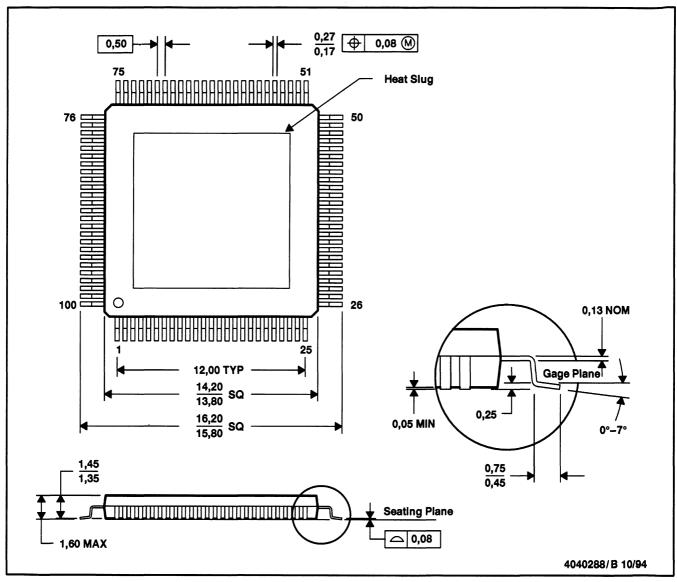
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)

PCA (S-PQFP-G100)

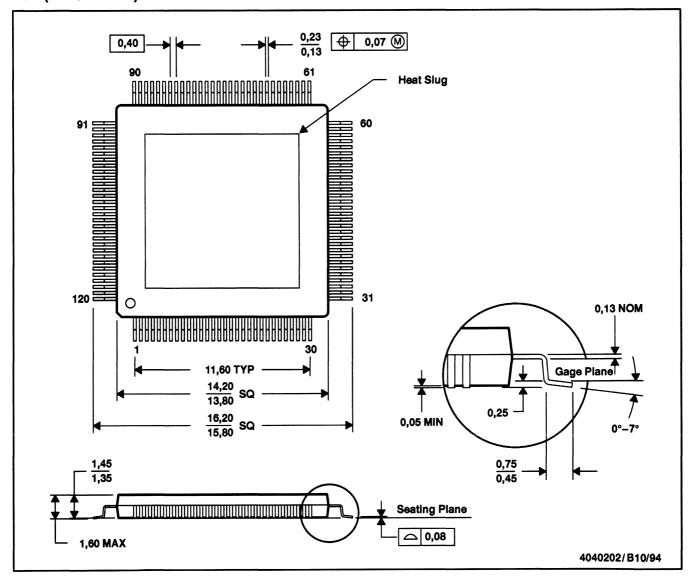
PLASTIC QUAD FLATPACK (DIE-DOWN)



- B. This drawing is subject to change without notice.
- C. Thermally enhanced molded plastic package with a heat slug (HSL)
- D. Falls within JEDEC MO-136

PCB (S-PQFP-G120)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-136
 - D. Thermally enhanced molded plastic package with a heat slug (HSL)

General Information	1
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Ceramic Surface-Mount	4
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PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
PDIP (PLASTIC DUAL-IN-LINE PACKAGE)	8 14/16/20 16/20 24/28 28	300 MIL	P N NE NT NP	4040082 4040049 4040054 4040050 4040075	3–5 3–6 3–7 3–8 3–9
	22/24 22	400 MIL	N NK	4040051 4040153	3–10 3–11
	24/28/32/40/48/52 24/28/40/48	600 MIL	N NW	4040053 4040079	3–12 3–13
	64	900 MIL	N	4040080	3–14
SDIP (SHRINK DUAL-IN-LINE PACKAGE)	22 24	300 MIL	NN NN	4040032-2 4040032-3	3–15 3–16
	28 30	400 MIL	NF NF	4040033 4040057	3–17 3–18
	40/54	600 MIL	NJ	4040034	3–19
	64	750 MIL	NM	4040056	3–20
TO/SOT (CYLINDRICAL PACKAGE)	2 3 3 3	TO-92	LP LP LPB LPF	4040248 4040001 4073350 4040249	3–21 3–22 3–23 3–24
	3	SOT-82	LL	4040235	3-25
	3 5 5 7 7	TO-220	KPA KC KC KV KC KV	4040252 4040207 4040208 4040209 4040251 4040233	3–26 3–27 3–28 3–29 3–30 3–31
	3	SOT-93	KCB	4040290	3–32
PFM (PLASTIC FLANGE-MOUNT PACKAGE)	3 (In Development) 3 (In Development) 5 (In Development) 5 (In Development) 7 (In Development) 7 (In Development) 7 (In Development) 9 9 (In Development) 9 (In Development) 15 15 (In Development)	CUSTOM	KTE KTF KTG KTH KTJ KTK KTL KTM KFA KGC KTA KTB KN KTC KTD	4073375 4073376 4073377 4073378 4073380 4073381 4073382 4040205 4040205 4040291 4073383 4073384 4040203 4073385 4073386	3-33 3-34 3-35 3-36 3-37 3-38 3-39 3-40 3-41 3-42 3-43 3-44 3-45 3-46 3-47
	8 8 15 15 15	JEDEC	KWV KW KV KVS KVA	4040199 4040198 4040210 4040204 4040003	3–48 3–49 3–50 3–51 3–52



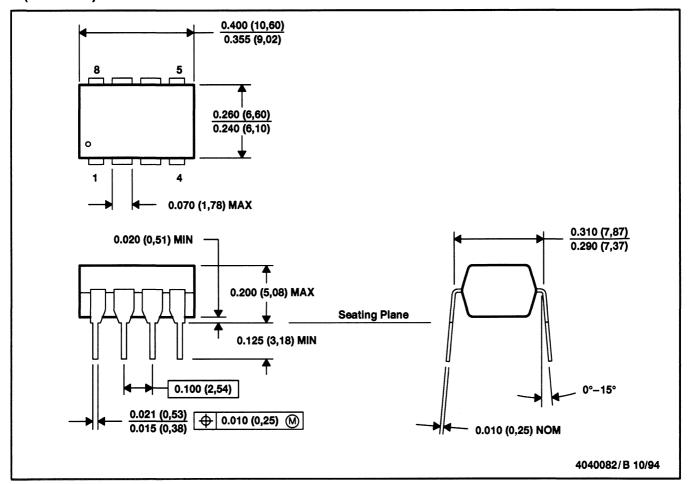
PLASTIC THROUGH-HOLE

CONTENTS

PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
SIP	2		SL	4040253-2	3-53
(SINGLE IN-LINE PACKAGE)	3		SL	4040253-3	3-54
	3		SLL	4040254	3–55
	4		SC	4040190-2	3-56
	4		SE	4040255	3-57
	4	1	SP	4040188	3–58
	7		SK	4040292	3-59
	10		SC	4040190-3	3–60
	14		SM	4040189	3–61
HSIP (THERMALLY ENHANCED)	3		PK	4040234	3–62
ZIP (ZIG-ZAG PACKAGE)	20/24/28		SD	4040206	3–63
ОРТО	3		SR	4040293	3-64
(LIGHT SENSOR PACKAGE)	8		NU	4040294	3-65

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

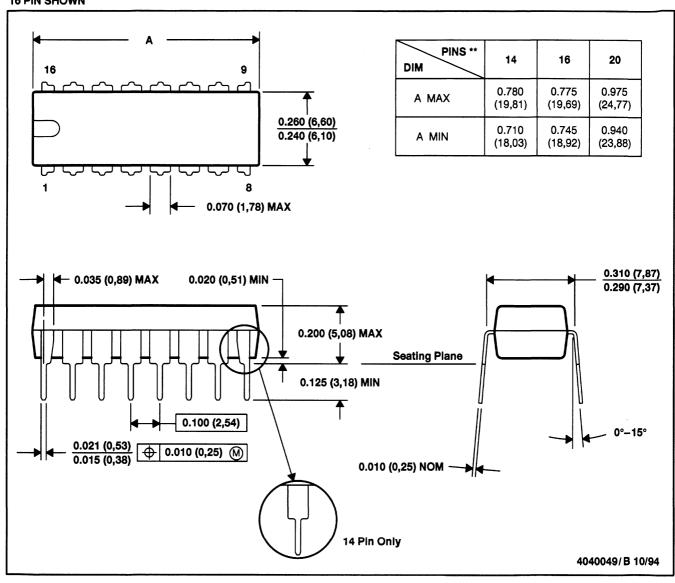


- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

N (R-PDIP-T**)

16 PIN SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

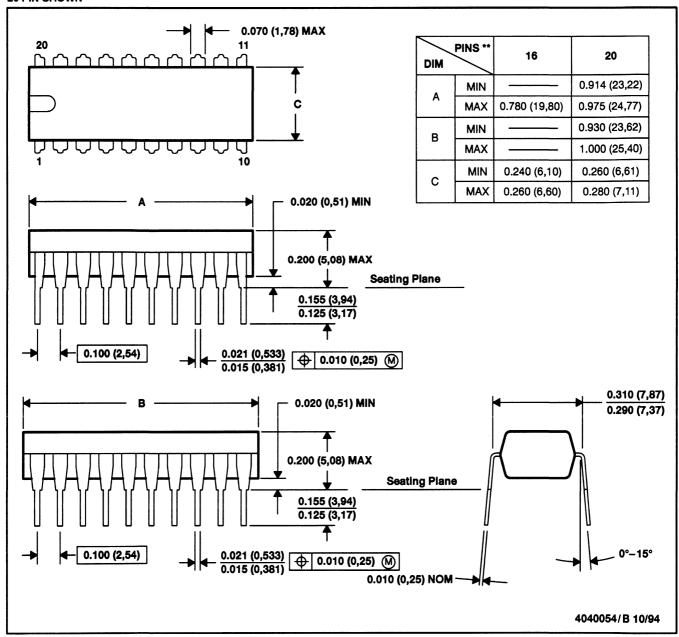
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001 (20-pin package is shorter then MS-001)

NE (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN



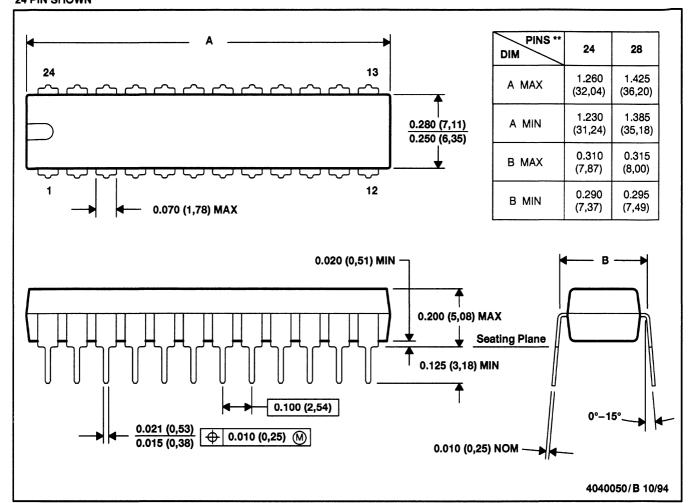
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 (16 pin only)

OCTOBER 1994

NT (R-PDIP-T**)

24 PIN SHOWN

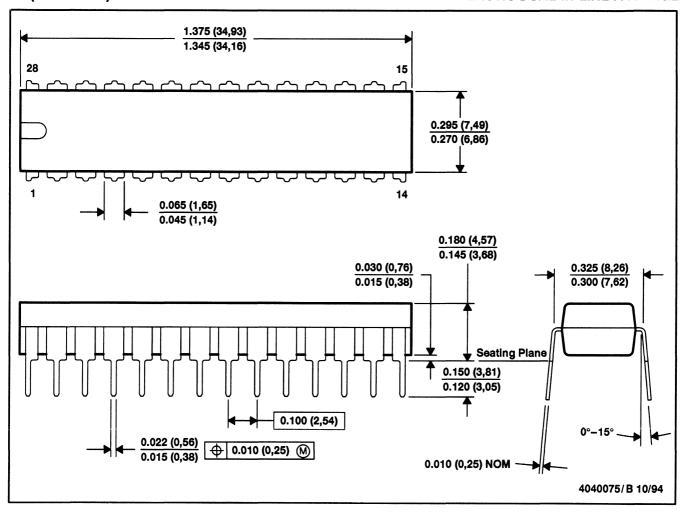
PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

NP (R-PDIP-T28)

PLASTIC DUAL-IN-LINE PACKAGE



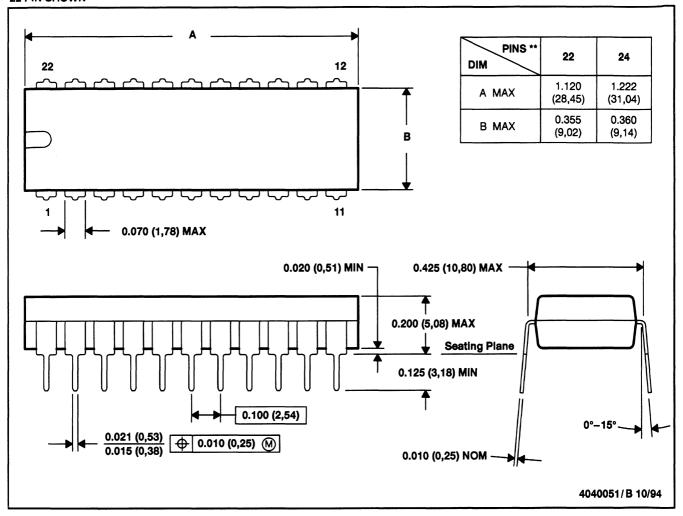
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-095

OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

22 PIN SHOWN



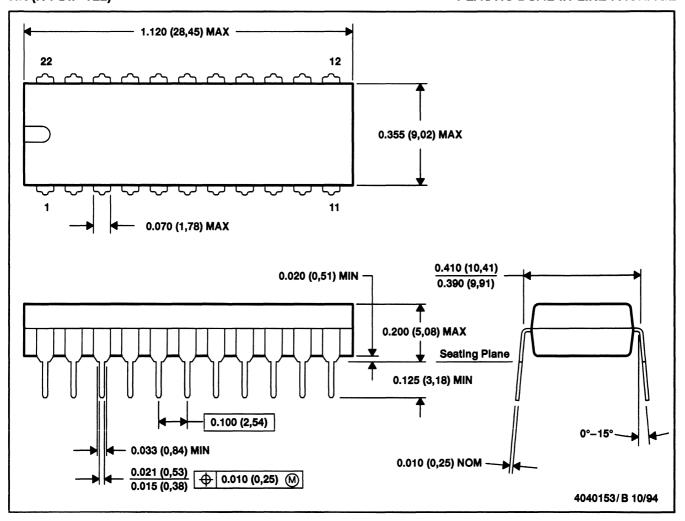
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-010

NK (R-PDIP-T22)

PLASTIC DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-010

OCTOBER 1994

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE 24 PIN SHOWN 0.560 (14,22) 0.520 (13,21) 12 - 0.060 (1,52) TYP 0.200 (5,08) MAX 0.610 (15,49) 0.590 (14,99) 0.020 (0,51) MIN **Seating Plane** 0.100 (2,54) 0.125 (3,18) MIN 0°-15° 0.015 (0,38) 0.010 (0,25) NOM PINS ** 24 28 32 40 48 52 DIM 2.650 1.450 1.650 2.090 2.450 1.270 A MAX (36,83)(41,91)(53,09)(62,23)(67,31)(32,26)2.390 2.590 1.230 1.410 1.610 2.040

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

A MIN

(31,24)

(35,81)

(40,89)

(51,82)

- C. Falls within JEDEC MS-011
- D. Falls within JEDEC MS-015 (32 pin only)

(65,79)

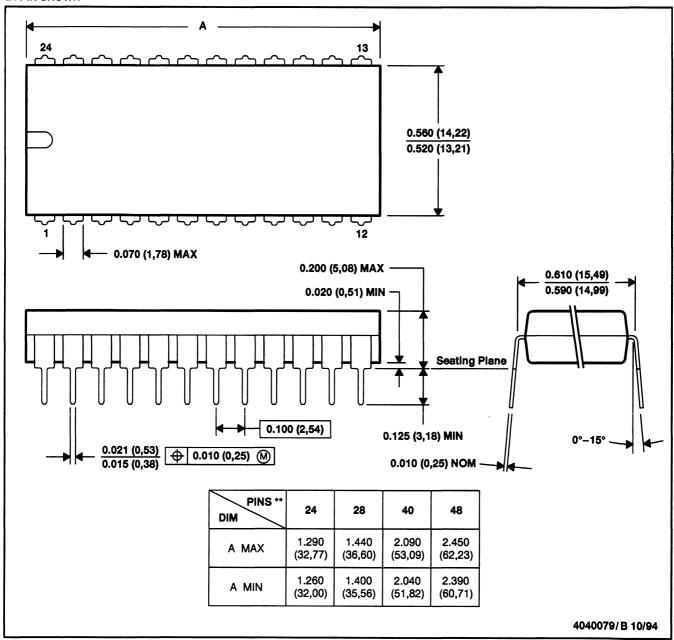
4040053/B 10/94

(60,71)

NW (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

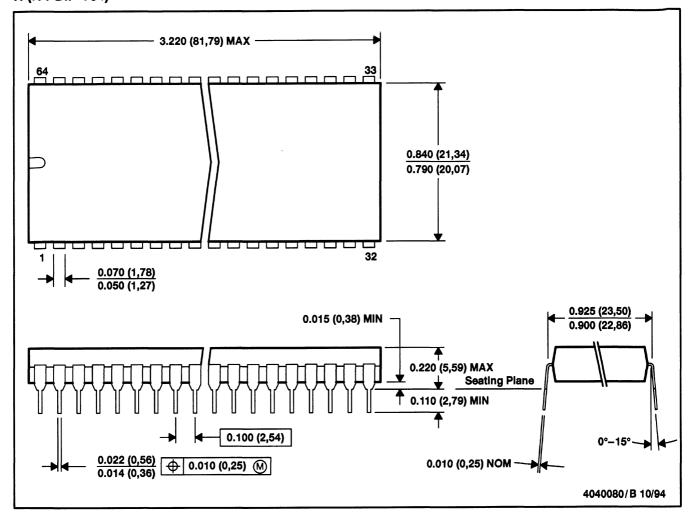
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-011

OCTOBER 1994

N (R-PDIP-T64)

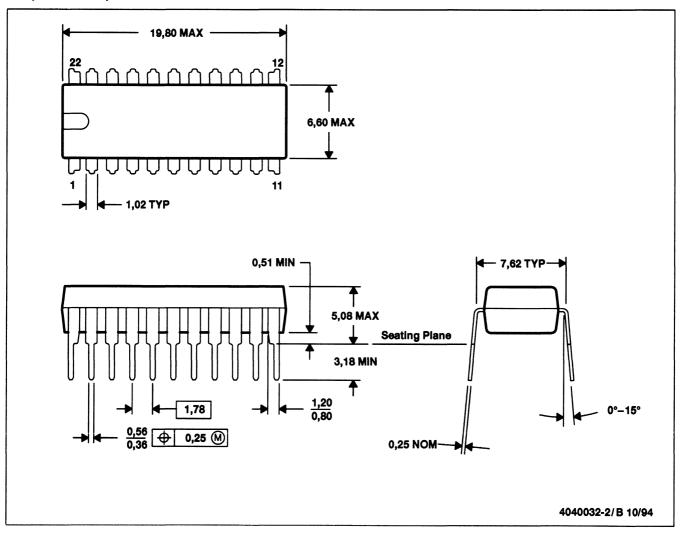
PLASTIC DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-016

NN (R-PDIP-T22)

PLASTIC SHRINK DUAL-IN-LINE PACKAGE



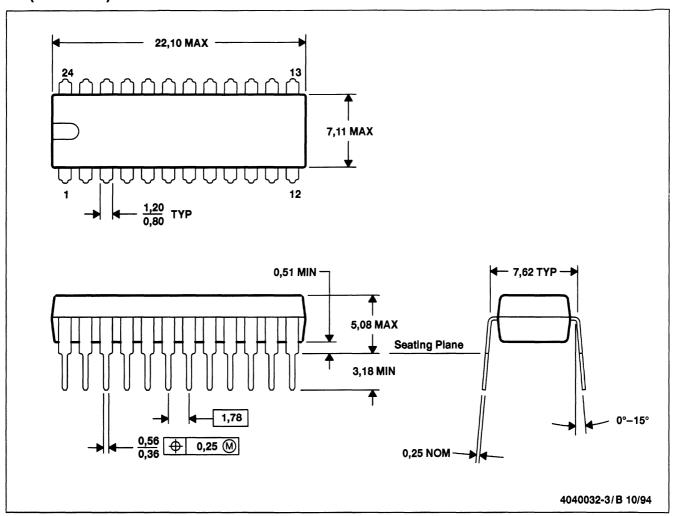
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions include mold flash or protrusion.

NN (R-PDIP-T24)

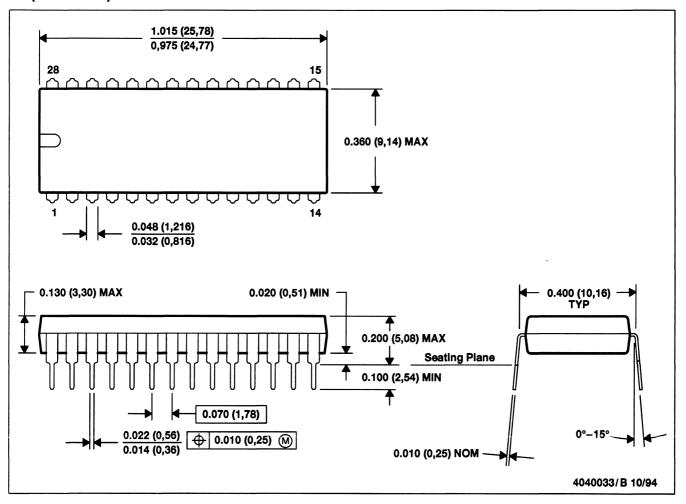
PLASTIC SHRINK DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

NF (R-PDIP-T28)

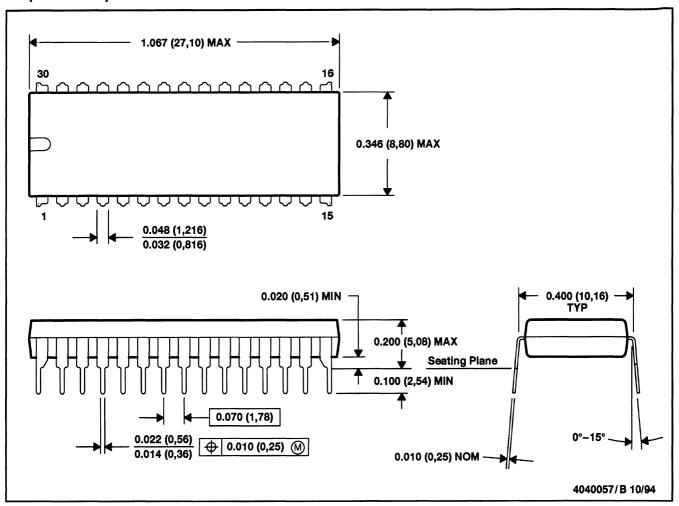
PLASTIC SHRINK DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

NF (R-PDIP-T30)

PLASTIC SHRINK DUAL-IN-LINE PACKAGE

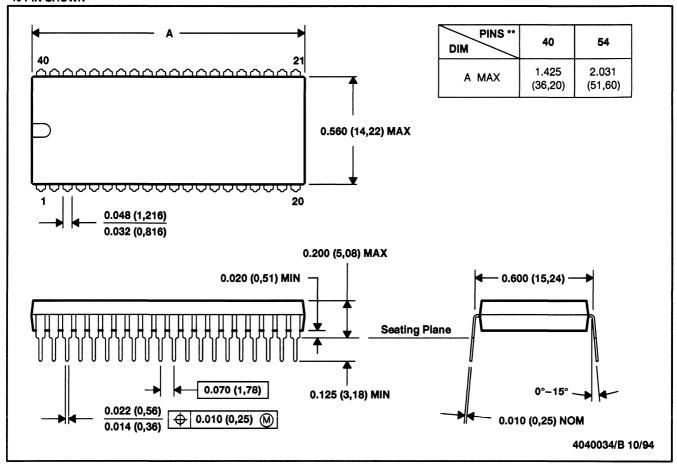


NOTES: A. All linear dimensions are in inches (millimeters).

NJ (R-PDIP-T**)

PLASTIC SHRINK DUAL-IN-LINE PACKAGE

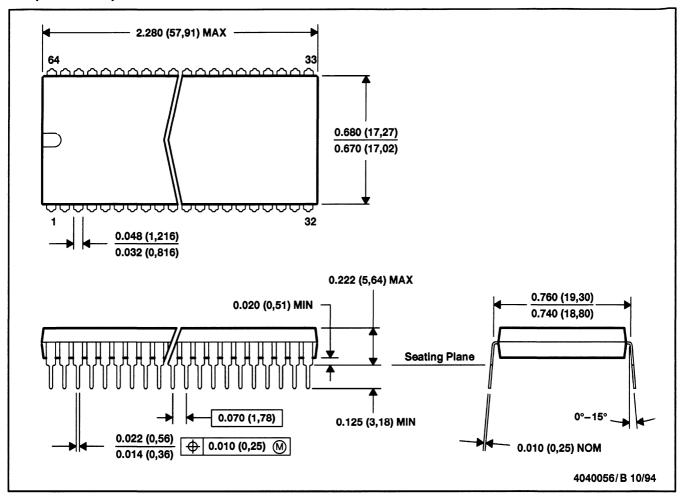
40 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

NM (R-PDIP-T64)

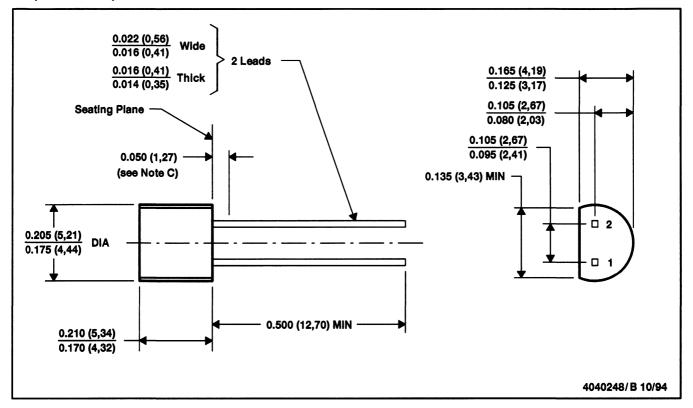
PLASTIC SHRINK DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

LP (O-PBCY-W2)

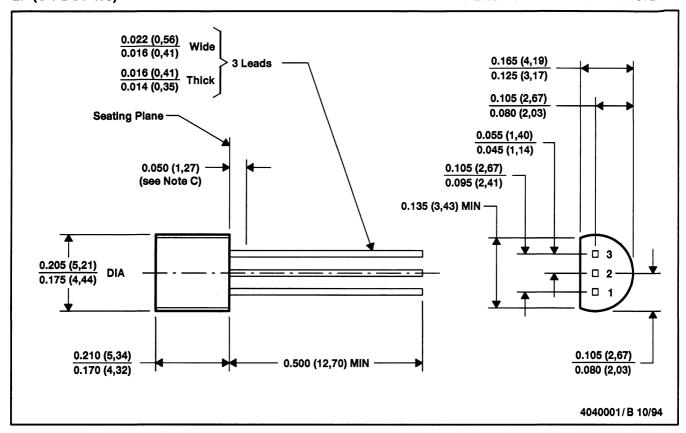
PLASTIC CYLINDRICAL PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. Falls within JEDEC TO-226AC (TO-226AC replaces TO-92)

LP (O-PBCY-W3)

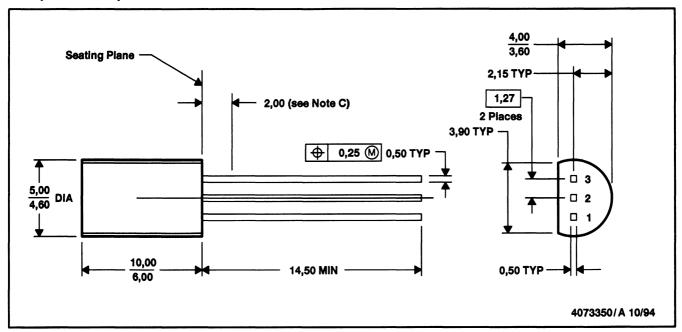
PLASTIC CYLINDRICAL PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. Falls within JEDEC TO-226AA (TO-226AA replaces TO-92)

LPB (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE

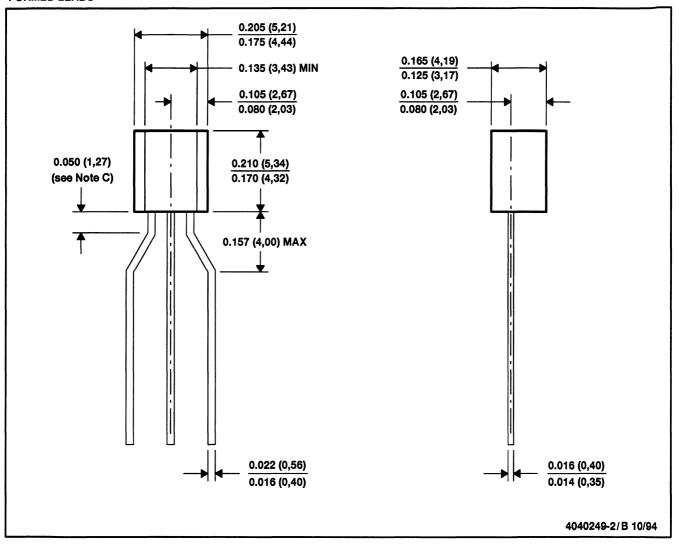


- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.

LPF (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE

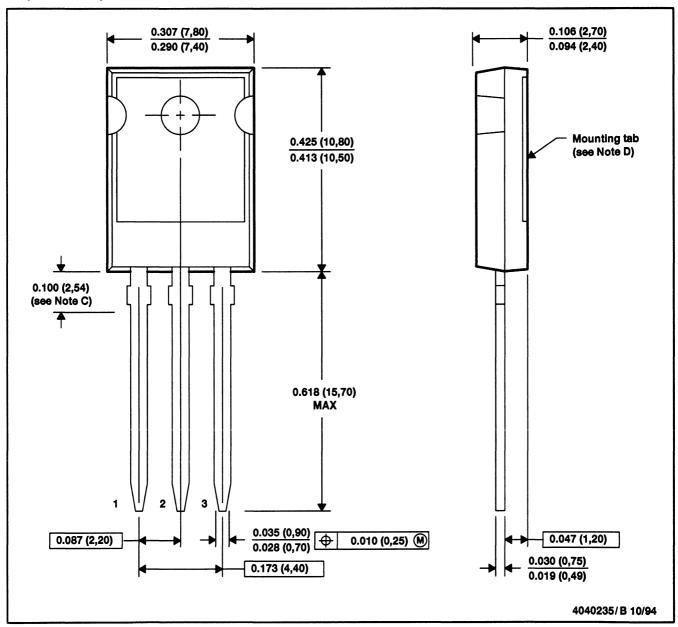
FORMED LEADS



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.

LL (R-PSFM-T3)

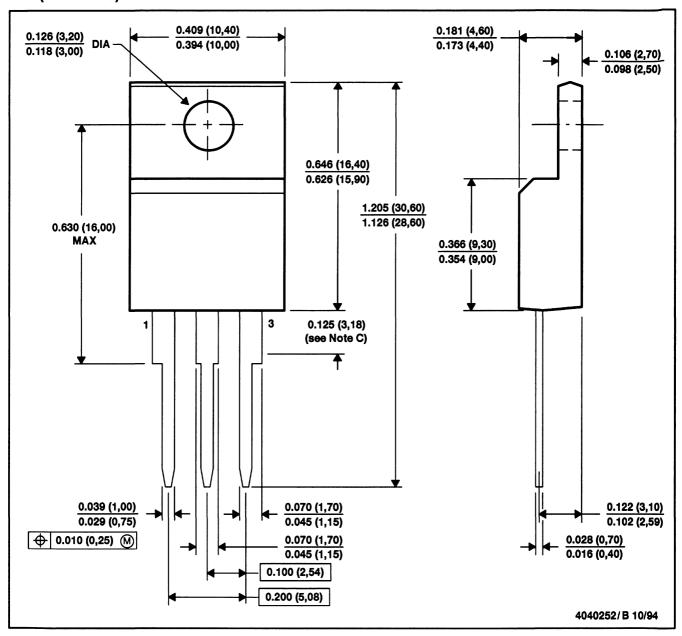
PLASTIC CLIP-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. The center lead is in electrical contact with the exposed mounting tab.
- E. All lead dimensions apply before solder dip.

KPA (R-PSFM-T3)

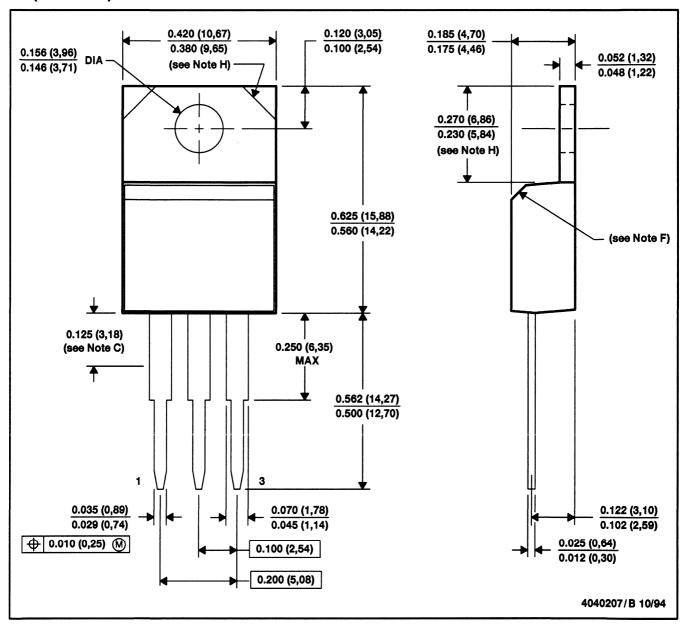
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The mounting tab is isolated.

KC (R-PSFM-T3)

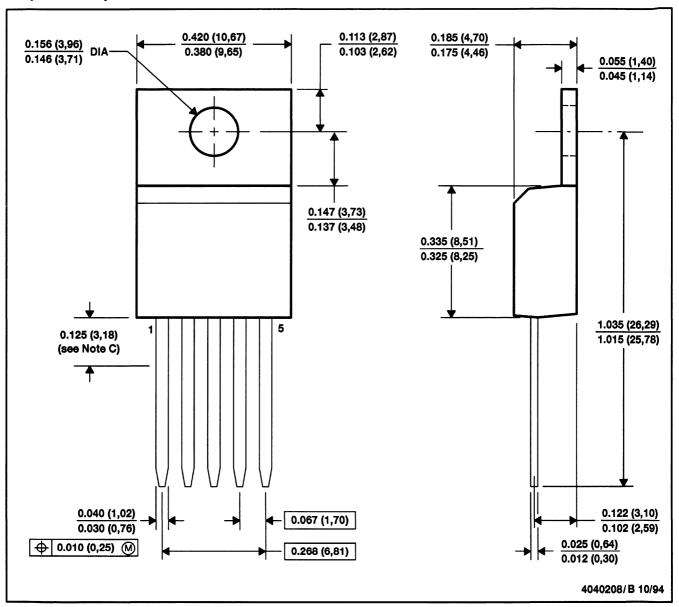
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Falls within JEDEC TO-220AB
- H. Tab contour optional within these dimensions

KC (R-PSFM-T5)

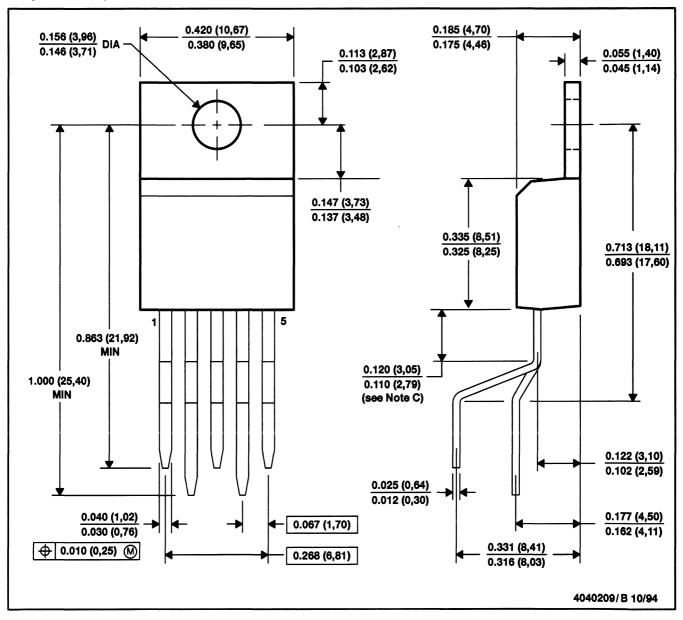
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.

KV (R-PZFM-T5)

PLASTIC FLANGE-MOUNT PACKAGE

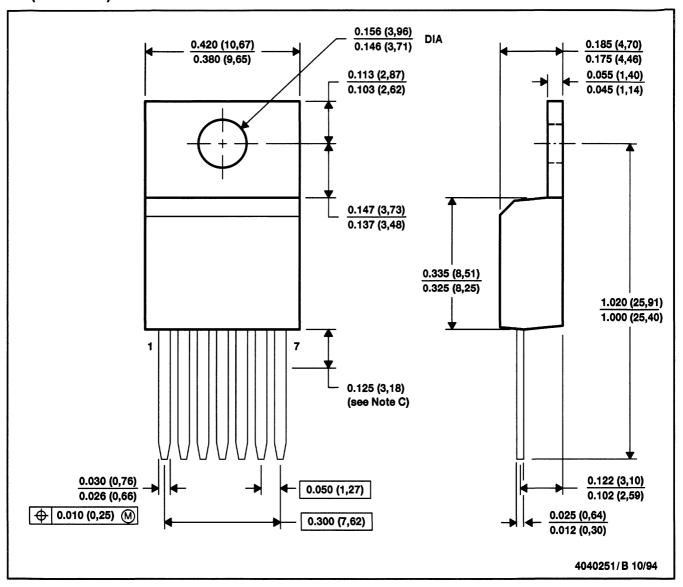


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.

KC (R-PSFM-T7)

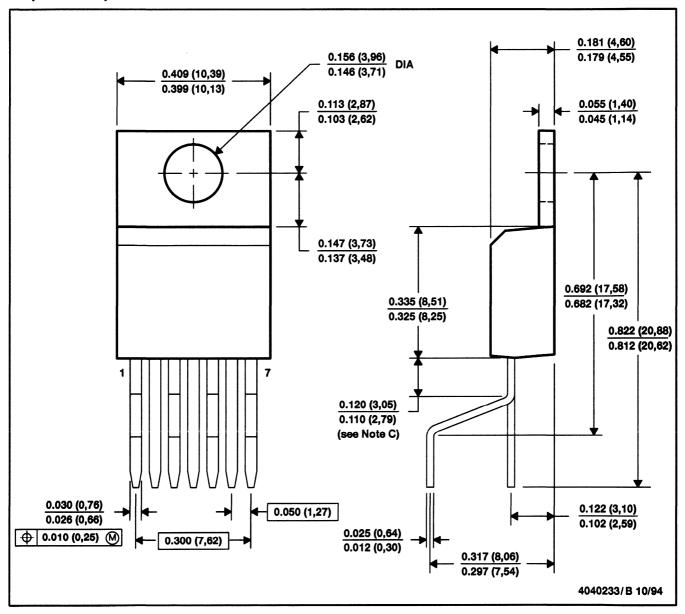
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.

KV (R-PZFM-T7)

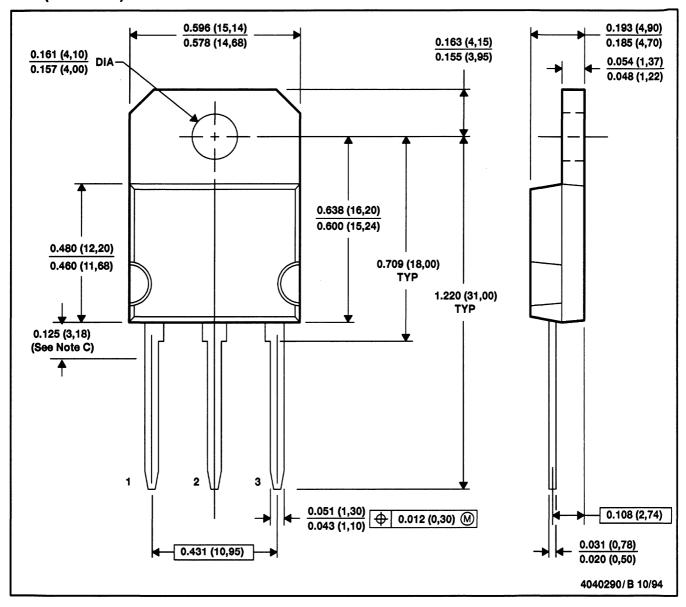
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area.
 - D. All lead dimensions apply before solder dip.

KCB (R-PSFM-T3)

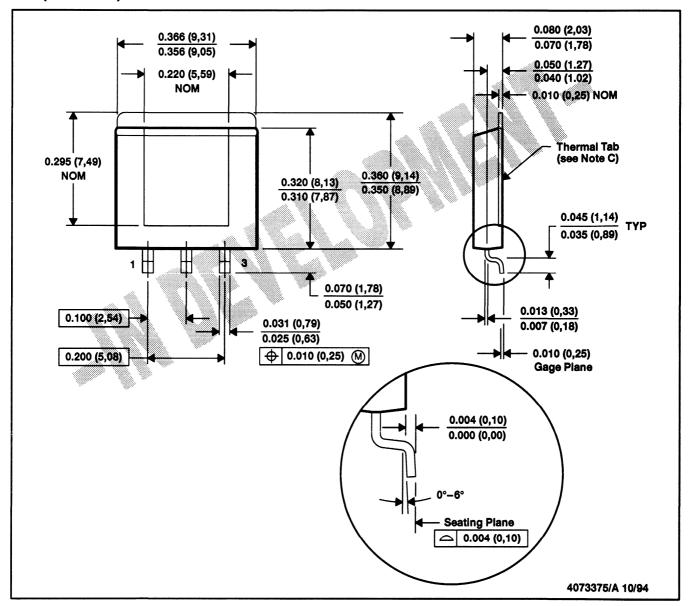
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.

KTE (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



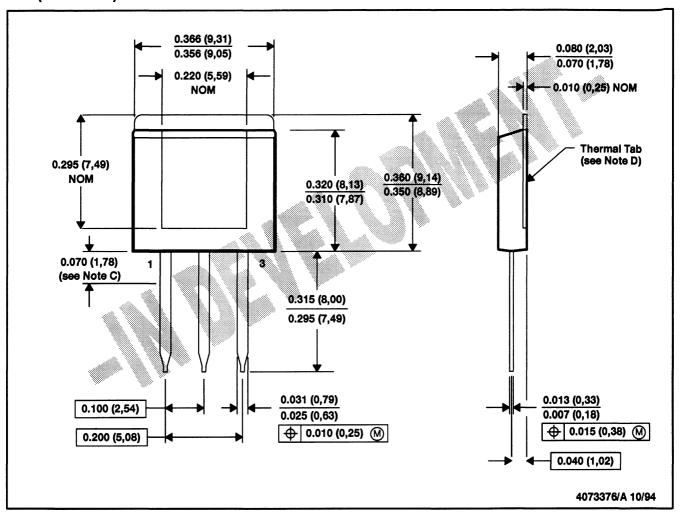
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. The center lead is in electrical contact with the thermal tab.

KTF (R-PSFM-T3)

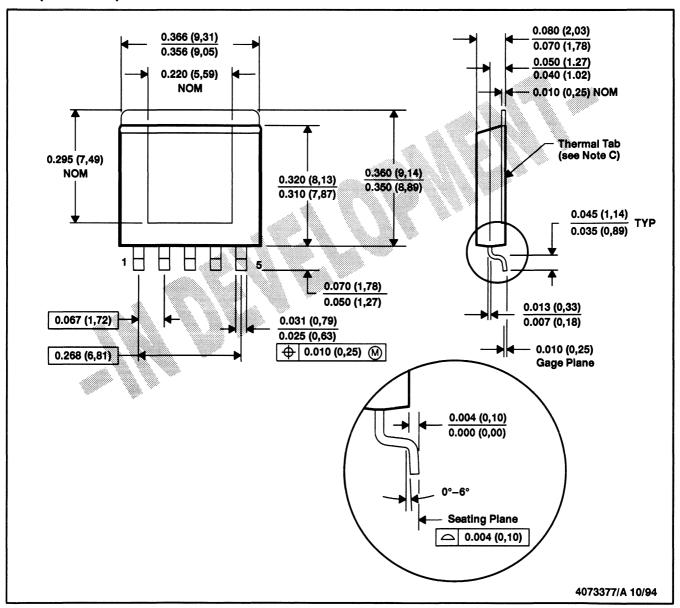
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead width not controlled in this area.
- D. The center lead is in electrical contact with the thermal tab.

KTG (R-PSFM-G5)

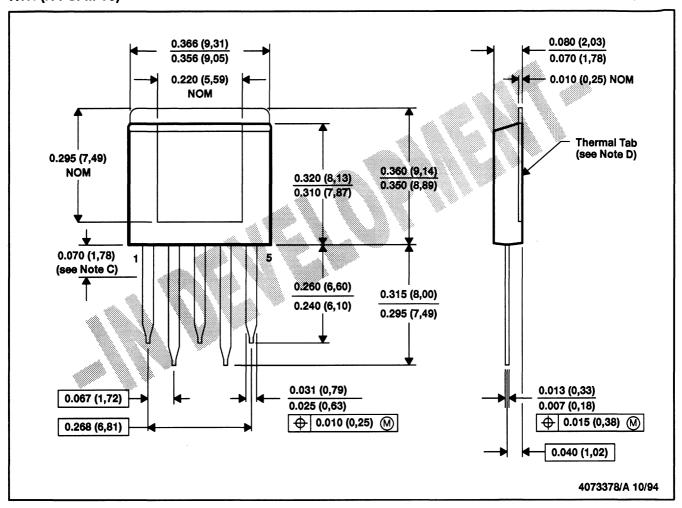
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the thermal tab.

KTH (R-PSFM-T5)

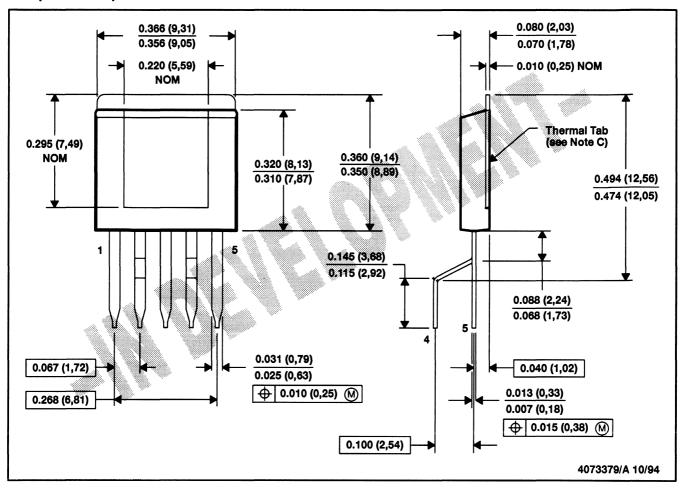
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead width not controlled in this area
- D. The center lead is in electrical contact with the thermal tab.

KTJ (R-PSFM-T5)

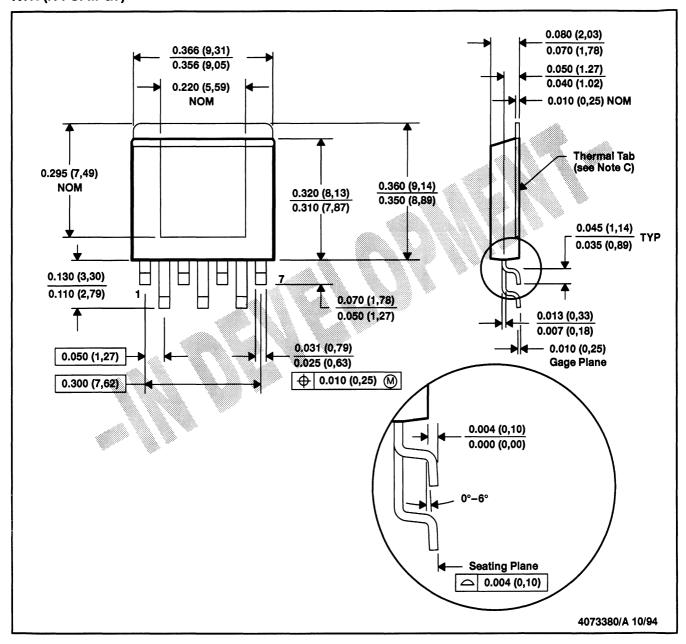
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the thermal tab.

KTK (R-PSFM-G7)

PLASTIC FLANGE-MOUNT PACKAGE



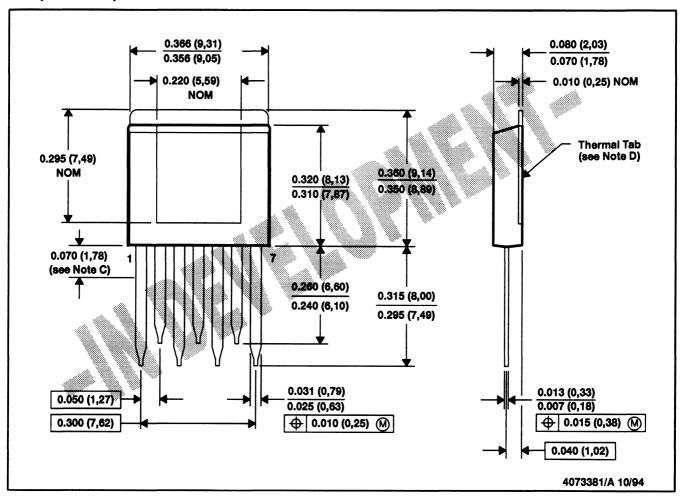
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. The center lead is in electrical contact with the thermal tab.

KTL (R-PSFM-T7)

PLASTIC FLANGE-MOUNT PACKAGE

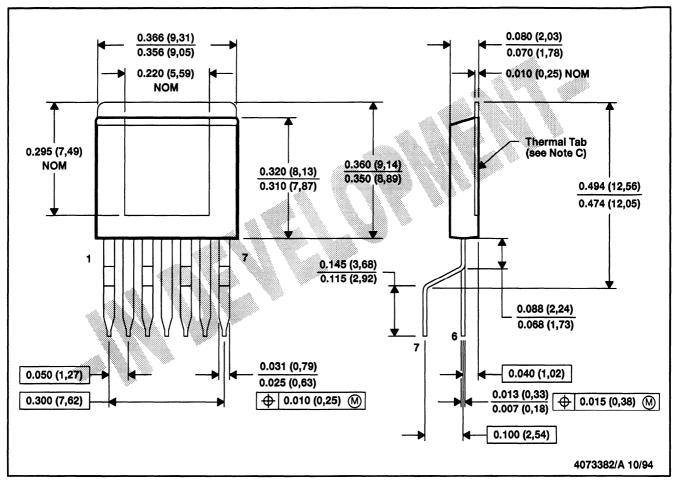


- B. This drawing is subject to change without notice.
- C. Lead width not controlled in this area
- D. The center lead is in electrical contact with the thermal tab.

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KTM (R-PSFM-T7)

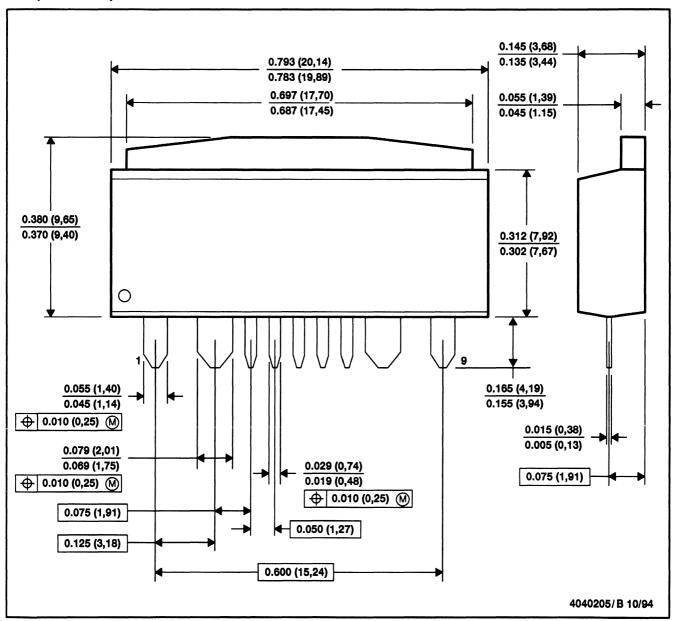
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the thermal tab.

KFA (R-PSFM-T9)

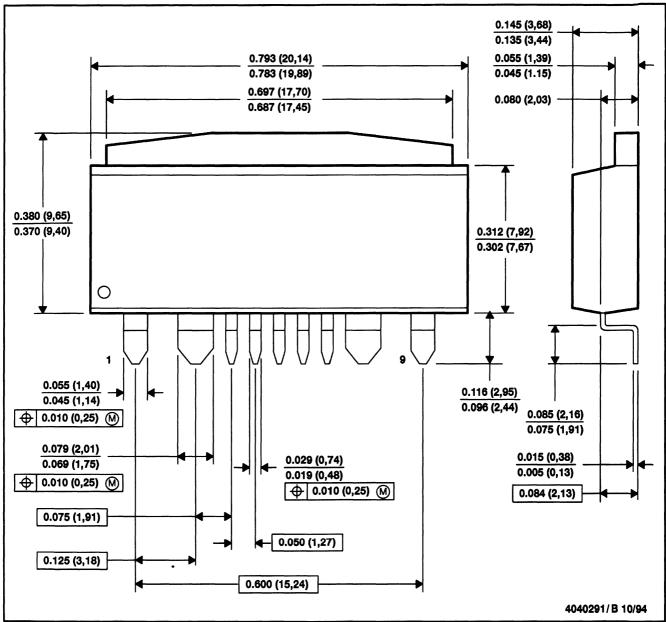
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. All lead dimensions apply before solder dip.
 - D. Leads 2 and 8 are in electrical contact with the mounting tab.

KGC (R-PSFM-G9)

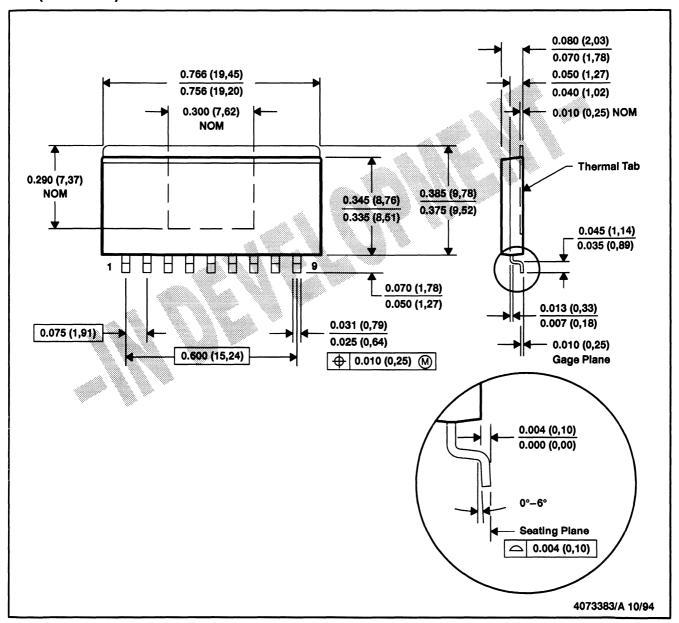
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. All dimensions apply before solder dip.
- D. Leads 2 and 8 are in electrical contact with the mounting tab.

KTA (R-PSFM-G9)

PLASTIC FLANGE-MOUNT PACKAGE

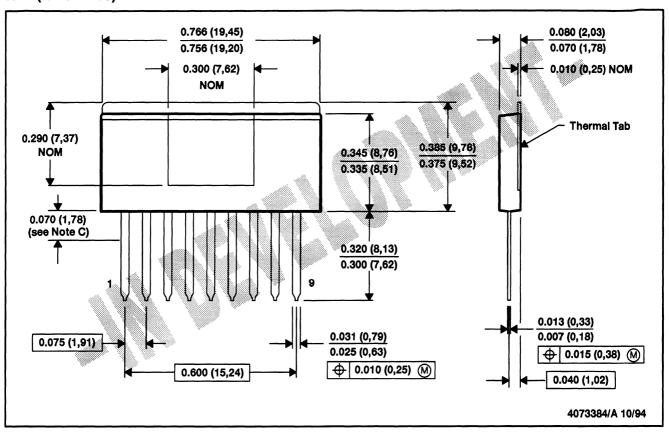


NOTES: A. All linear dimensions are in inches (millimeters).

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KTB (R-PSFM-T9)

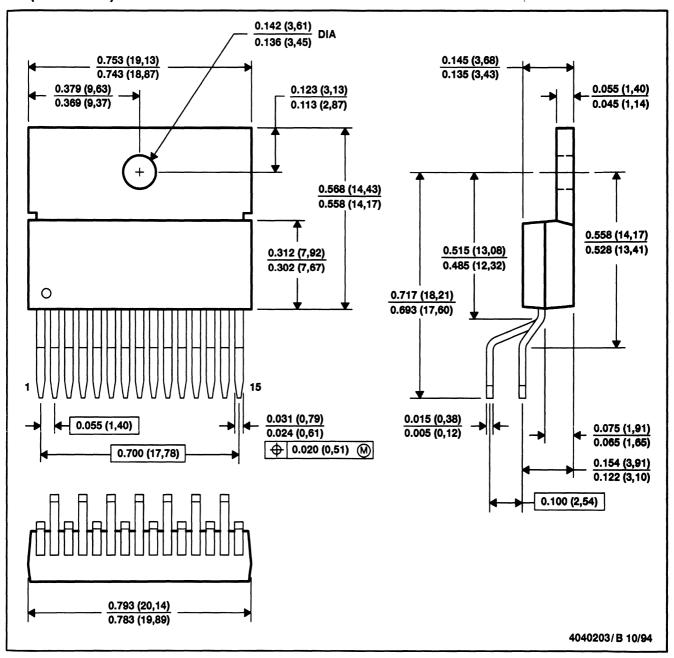
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead width not controlled in this area

KN (R-PZFM-T15)

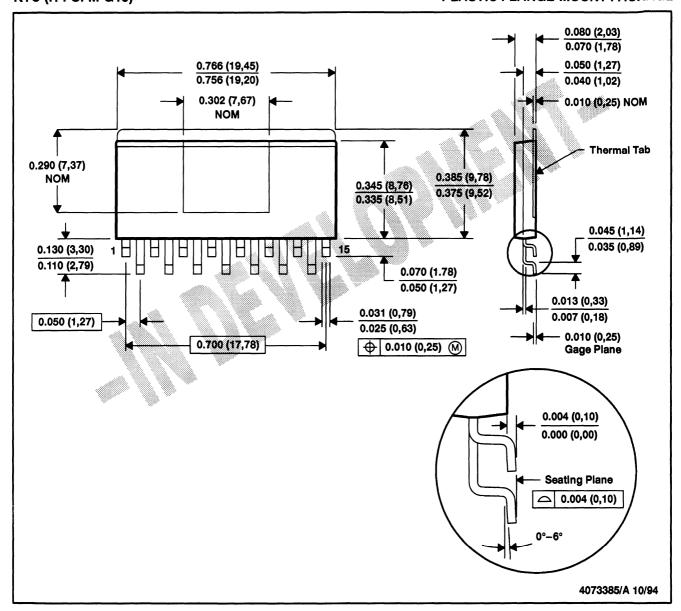
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. All lead dimensions apply before solder dip.

KTC (R-PSFM-G15)

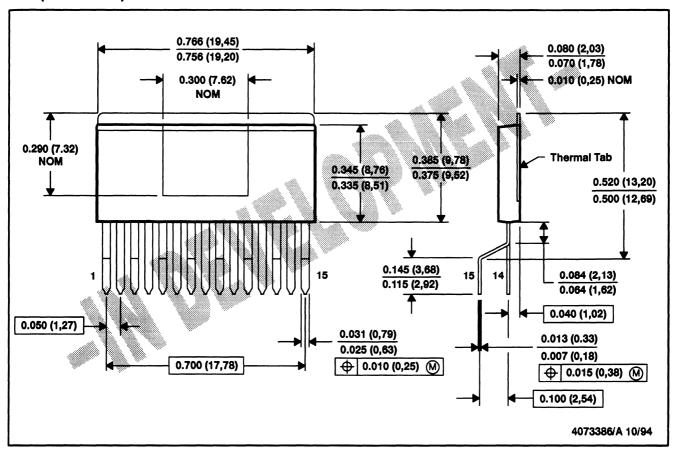
PLASTIC FLANGE-MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

KTD (R-PSFM-T15)

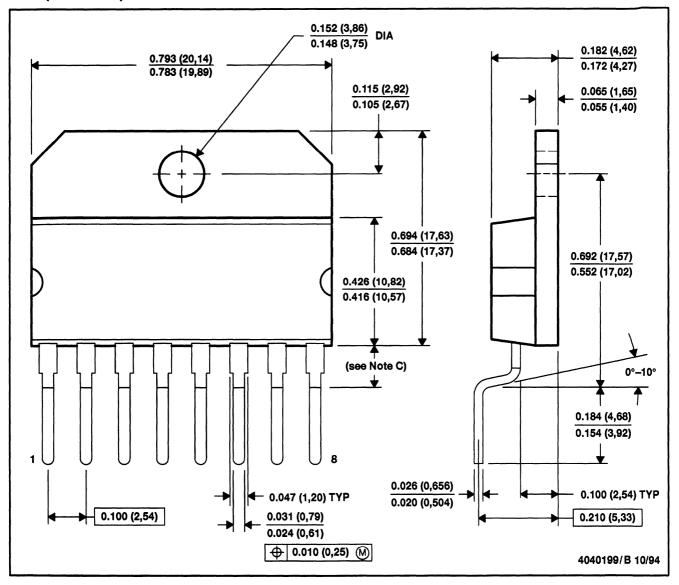
PLASTIC FLANGE-MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

KWV (R-PSFM-T8)

PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.

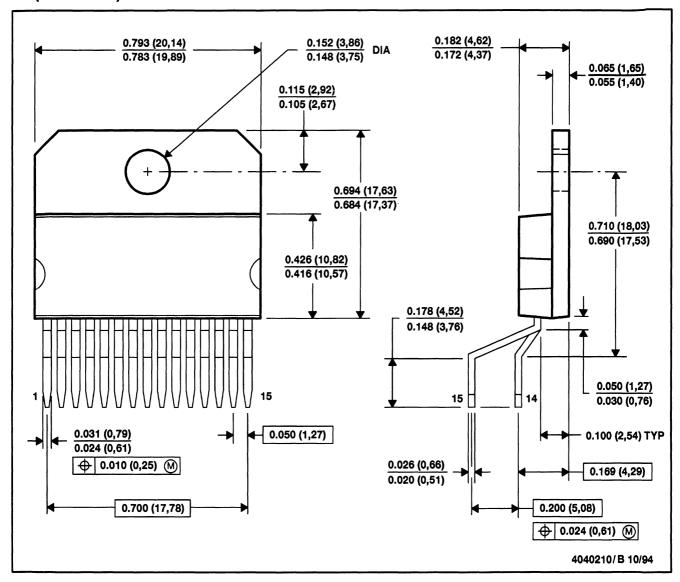
KW (R-PSFM-T8) PLASTIC FLANGE-MOUNT PACKAGE 0.182 (4,62) 0.172 (4,37) 0.793 (20,14) 0.065 (1,65) 0.783 (19,89) 0.055 (1,40) 0.514 (15,06) 0.504 (12,80) 0.426 (10,82) 0.416 (10,57) 0.622 (15,80) 0.583 (14,80) (see Note C) 土 0°-10° 0.184 (4,68) 0.154 (3,92) 0.026 (0,656) 0.047 (1,20) TYP 0.020 (0,504) 0.100 (2,54) 0.100 (2,54) TYP 0.031 (0,79) 0.024 (0,61) ⊕ 0.010 (0,25) M 0.210 (5,33) 4040198/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.

KV (R-PZFM-T15)

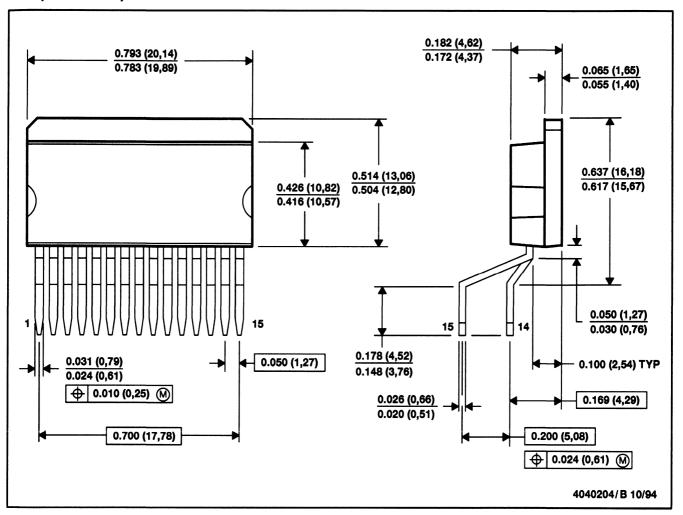
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. All lead dimensions apply before solder dip.
- D. Falls within JEDEC MO-048AB

KVS (R-PZFM-T15)

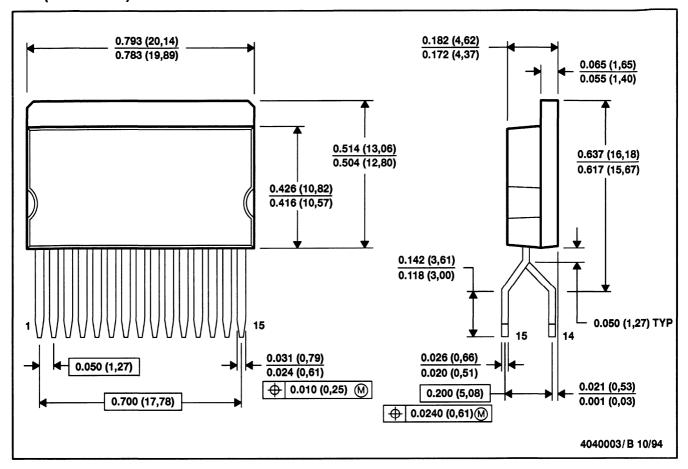
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. All lead dimensions apply before solder dip.

KVA (R-PZFM-T15)

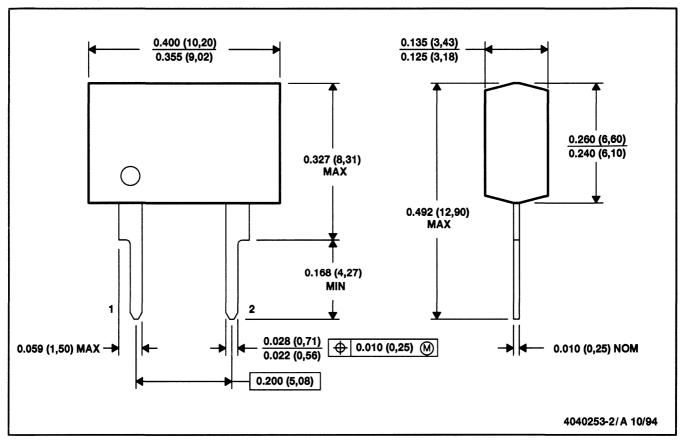
PLASTIC FLANGE-MOUNT PACKAGE



- B. This drawing is subject to change without notice.
- C. All lead dimensions apply before solder dip.

SL (R-PSIP-T2)

PLASTIC SINGLE-IN-LINE PACKAGE

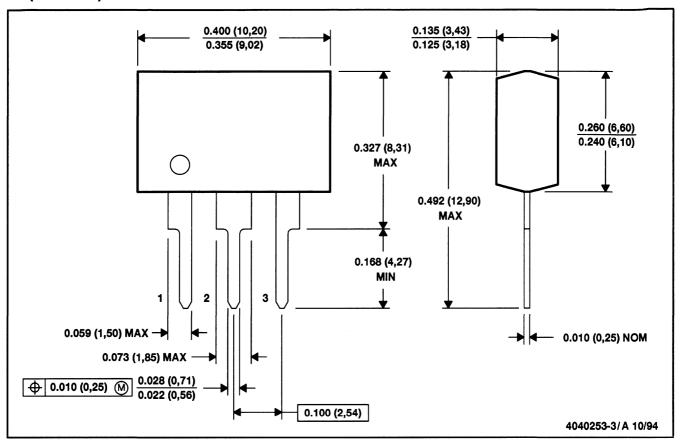


NOTES: A. All linear dimensions are in inches (millimeters).

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SL (R-PSIP-T3)

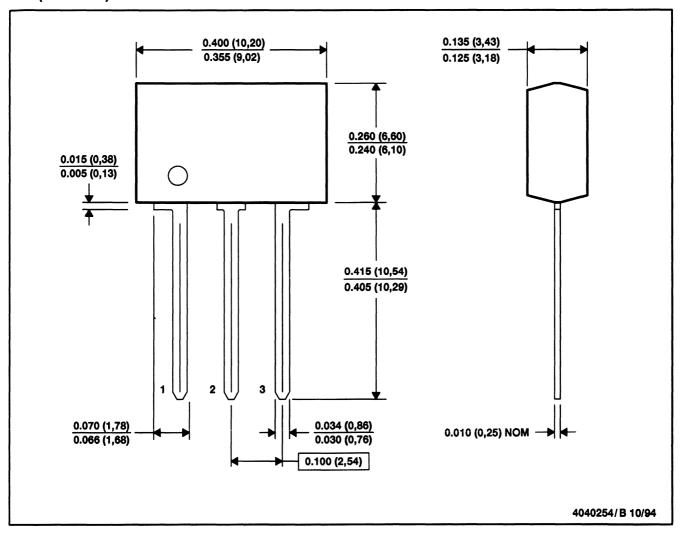
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SLL (R-PSIP-T3)

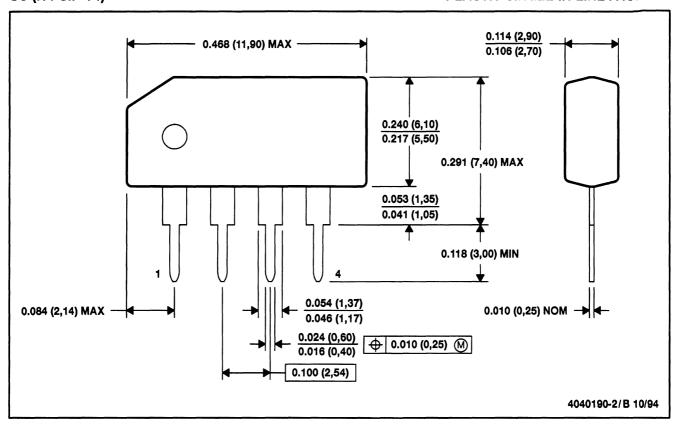
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SC (R-PSIP-T4)

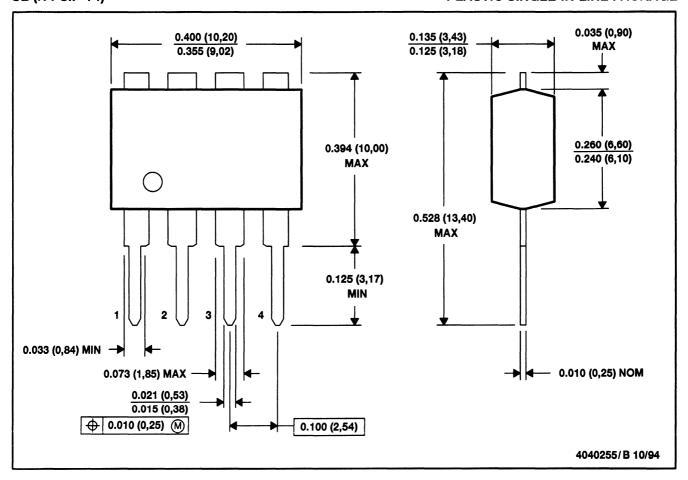
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SE (R-PSIP-T4)

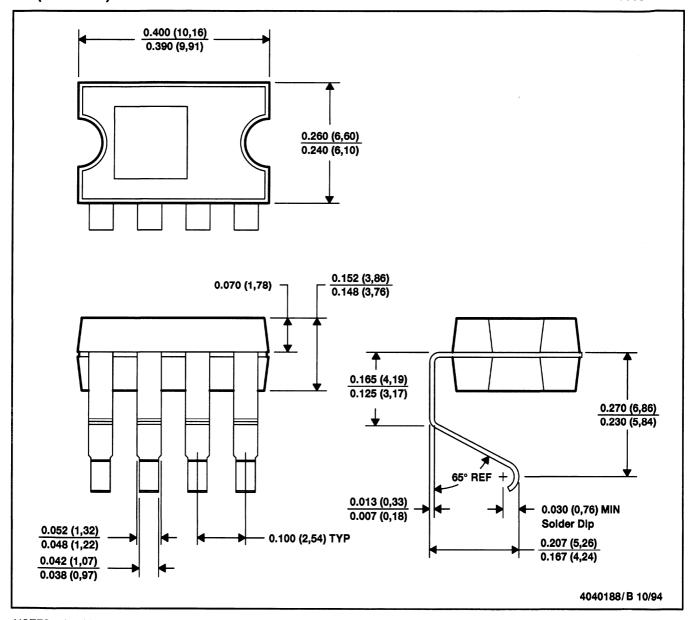
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SP (R-PSIP-T4)

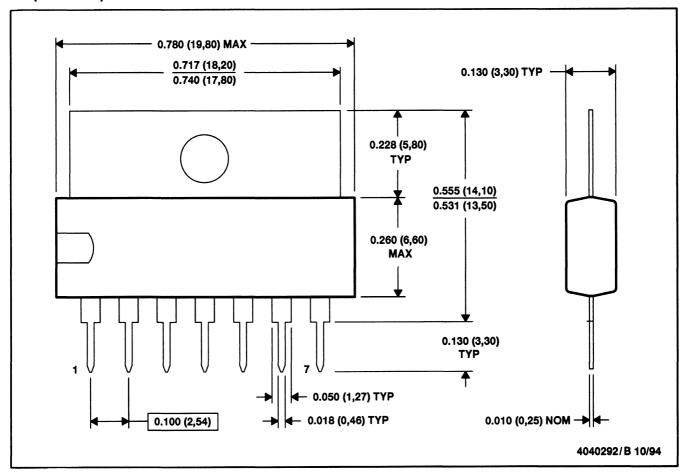
CUSTOM PHOTO-AMP PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SK (R-PSIP-T7)

PLASTIC SINGLE-IN-LINE PACKAGE

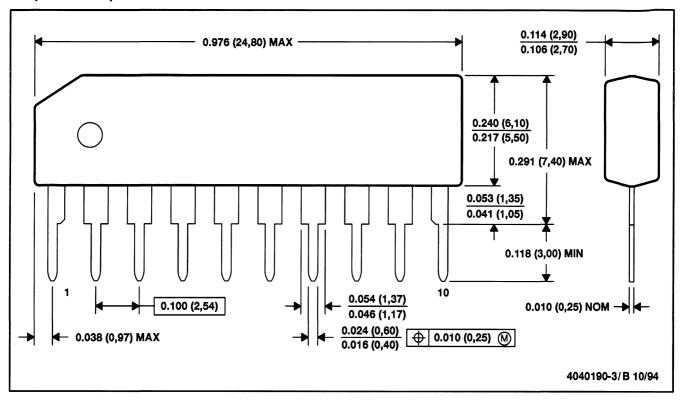


- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

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SC (R-PSIP-T10)

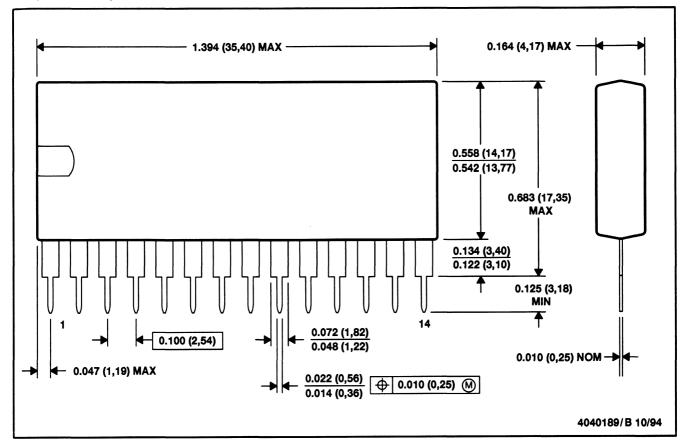
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

SM (R-PSIP-T14)

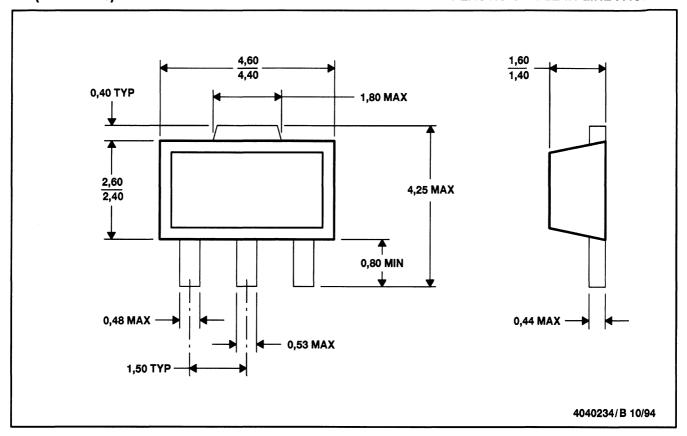
PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

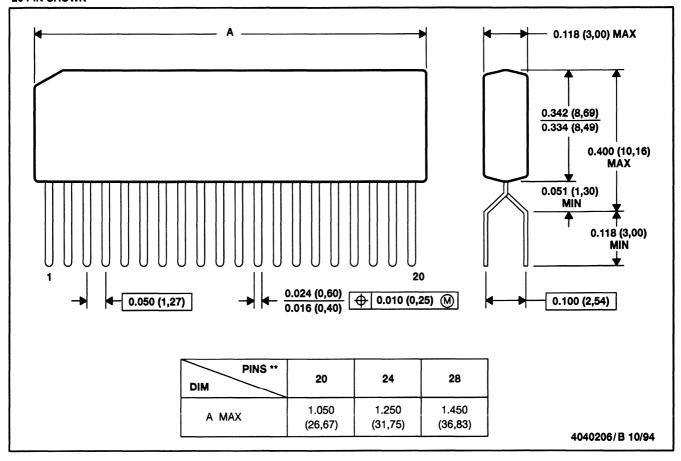
B. This drawing is subject to change without notice.

C. The center lead is in electrical contact with the tab.

SD (R-PZIP-T**)

PLASTIC ZIG-ZAG IN-LINE PACKAGE

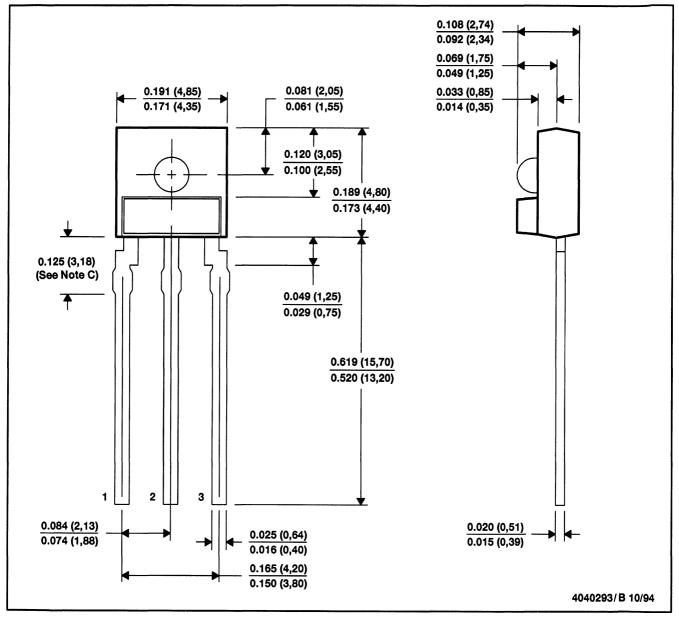
20 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

SR (R-PSIP-T3)

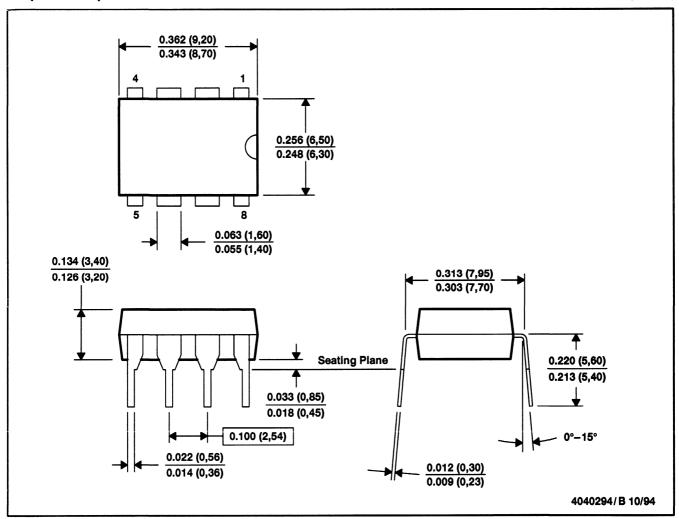
PLASTIC SINGLE-IN-LINE PACKAGE (OPTO)



- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All dimensions apply before solder dip.
- E. Package body is a clear nonfilled optically transparent material

NU (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE (OPTO)



- B. This drawing is subject to change without notice.
- C. All dimensions apply before solder dip.
- D. Package body is a clear non-filled optically transparent material.
- E. Optical center is determined by lead frame design.

General Information	1
Plastic Surface-Mount	2
Plastic Through-Hole	3
Ceramic Surface-Mount	4
Ceramic Through-Hole	5
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PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
JLCC	20		HJ	4040144-2	4–5
(J-LEADED CHIP CARRIER)	28		HJ	4040144-3	4–6
	28/44/68		FZ	4040219	4–7
	44/68		FJ	4040139	4–8
LCCC	18		FG	4040221	4–9
(LEADLESS CERAMIC CHIP	18		FV	4040141	4–10
CARRIER)	18/28/32		FE	4040137	4-11
·	20/28/44/52/68/84		FD	4040136	4–12
	20/28/44/52/68/84		FH	4040138	4–13
	20/28/44/52/68/84		FK	4040140	4–14
	20		FQ	4040143	4-15
	20		HL	4040145	4–16
	20		Інм	4040146-2	4–17
	24(28)		FNC	4040142	4–18
	28		НМ	4040146-3	4–19
CFP – UNFORMED	10	DUAL	U	4040179	4–20
(CERAMIC FLAT PACKAGE)	14	307.2	Ĭw	4040180-2	4-21
(02.17.11.10.10.10.10.10.10.10.10.10.10.10.10.	14		l wa	4040178	4-22
	16		w	4040180-3	4–23
	20		lнк	4040174	4-24
	20		lw`	4040180-4	4-25
	24		lŵ	4040180-5	4–26
	28		НКА	4040119	4–27
	28		нкв	4040120	4–28
	48/56		WD	4040176	4–29
	64		нкс	4073160	4–30
	68	QUAD	НВ	4040163	4–31
	68	GOAD	HV	4040072	4-32
	84		HFG	4040231-2	4–33
	84		HT	4040169-2	4–34
	100		HFG	4040231-3	4–35
	100		HS	4040071	4–36
	120		HBG	4073161	4-37
	132		HFG	4040231-4	4-38
	132		HT	4040169-3	4-39
	172		HFG		
			HT	4040231-5 4040169-4	4-40
	172 196		HFG		4-41
				4040231-6	4-42
	196		HT	4040169-5	4-43
	256		HFA	4040217	4-44
	256		HFH	4040232-2	4-45
	288		HFH	4040232-3	4–46
	320		HFH	4040232-4	4–47
	352		HFH	4040232-5	4–48

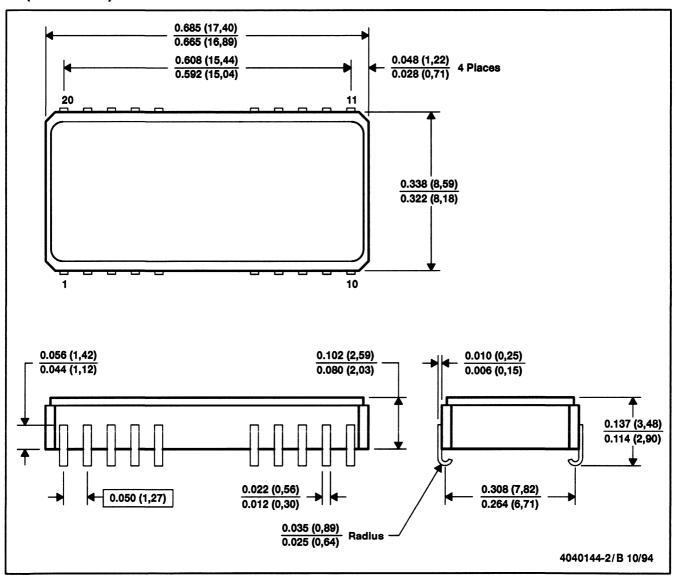
CERAMIC SURFACE-MOUNT

CONTENTS

PACKAGE	PINS	REMARKS	ID	DRAWING #	PAGE
CFP - FORMED	80	QUAD	HD	4040162	4-49
(CERAMIC FLAT PACKAGE)	96		HH	4073158	4–50
	100		HE	4040164	451
	128		HGA	4040118	4-52
	144/160		HP	4040117	4-53
	160		HY	4040112	4-54
	176		HZ	4040073	4-55
	196		HU	4040170	4–56
	208		HAF	4073163	4-57
	208	l	HPA	4040121	4–58
	208		WF	4040167	4–59
	240		HPC	4040113	4–60
	240		WG	4040227	4–61
	240		WH	4040168	4–62
	240		wĸ	4081525	4–63
	240		WM	4081526	464
	256		НВМ	4081527	4-65

HJ (R-CDCC-J20)

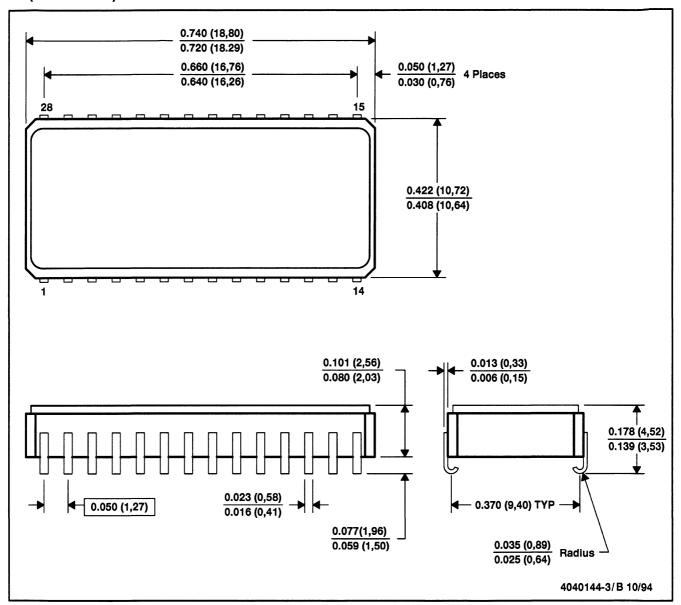
J-LEADED CERAMIC CHIP CARRIER



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.

HJ (R-CDCC-J28)

J-LEADED CERAMIC CHIP CARRIER

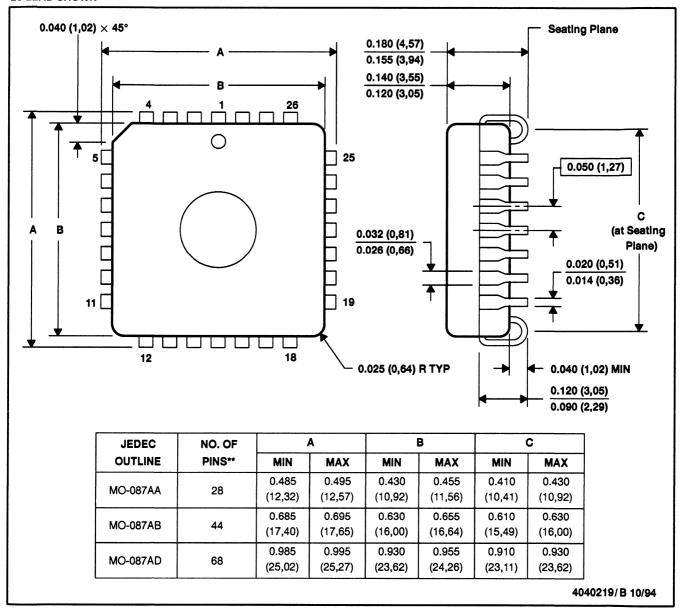


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



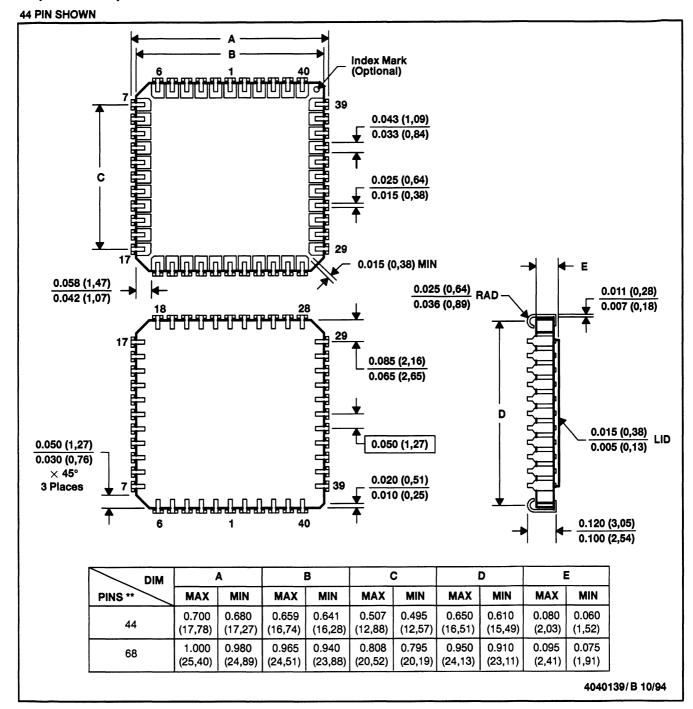
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

FJ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER



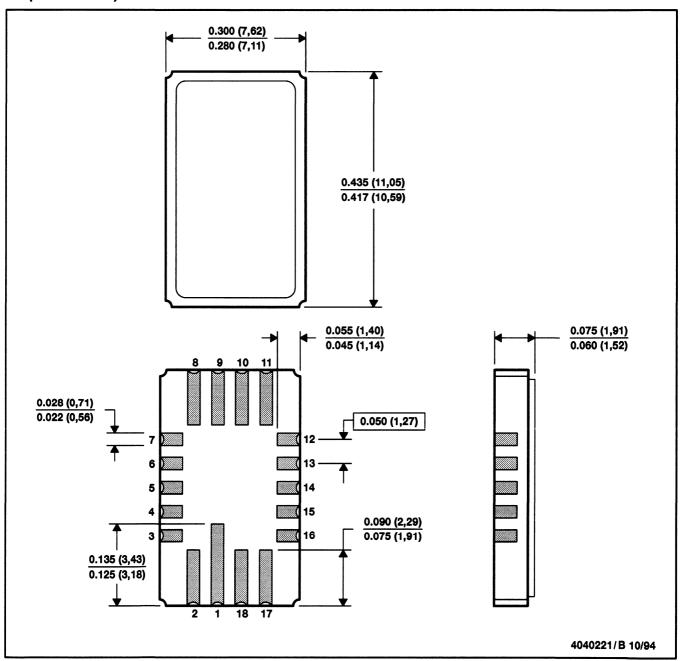
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Index mark may appear on top or bottom depending on package vendor

FG (R-CQCC-N18)

LEADLESS CERAMIC CHIP CARRIER

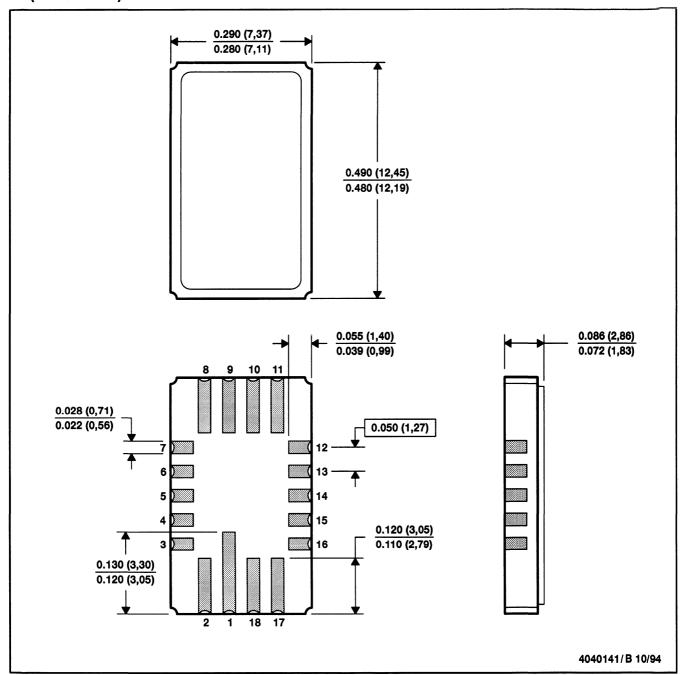


- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within MIL STD 1835 CQCC4-N18 and JEDEC MO-041AC



FV (R-CQCC-N18)

LEADLESS CERAMIC CHIP CARRIER



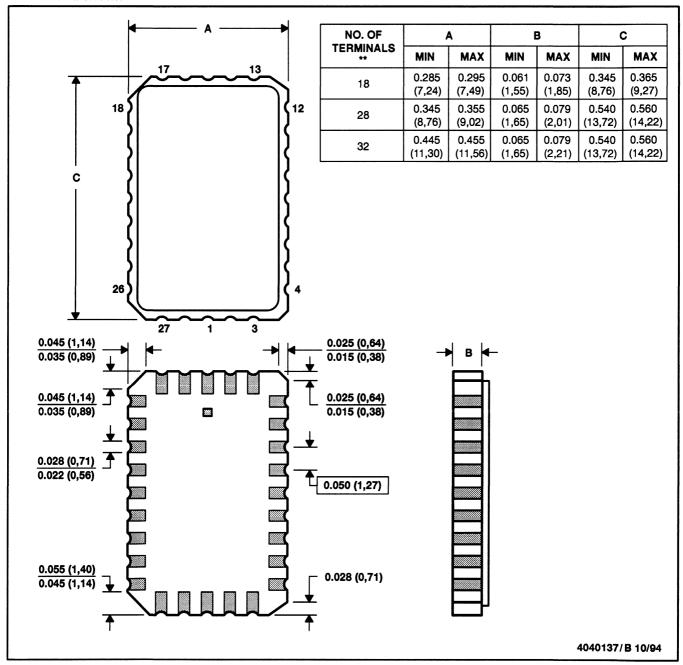
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

FE (R-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

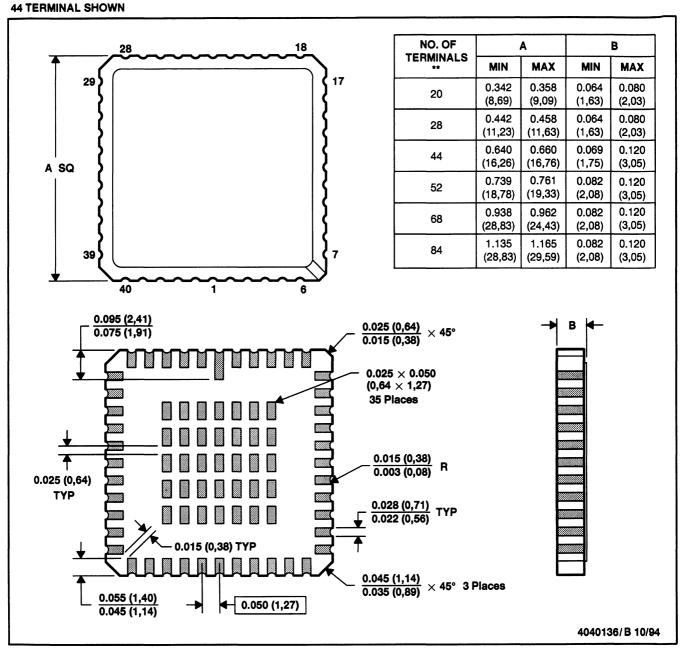


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.



FD (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

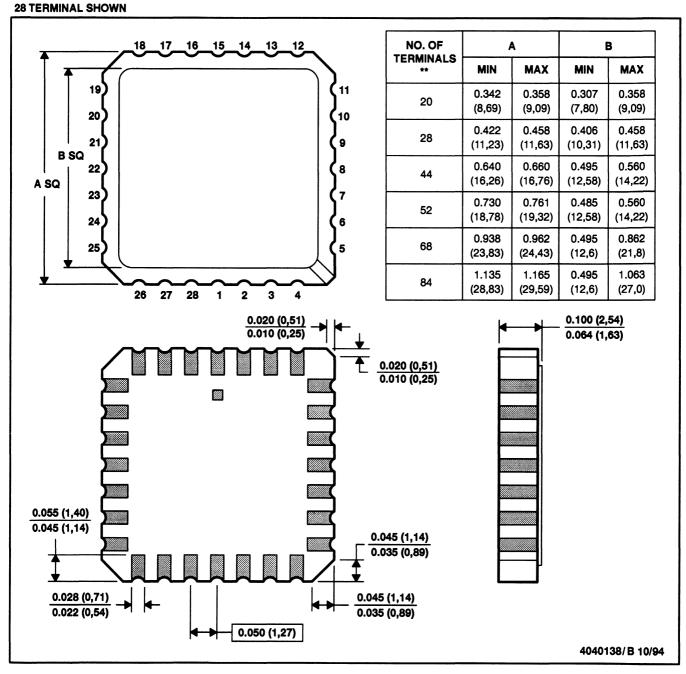


- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004



FH (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER



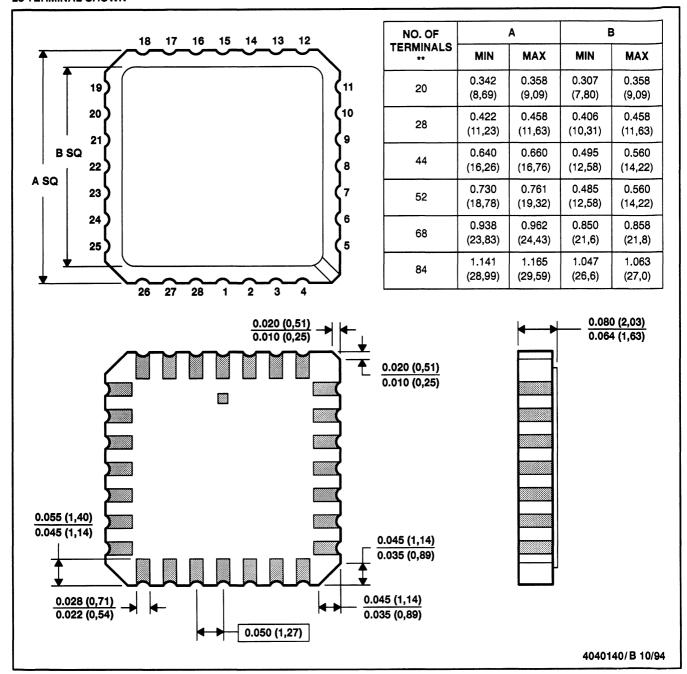
- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

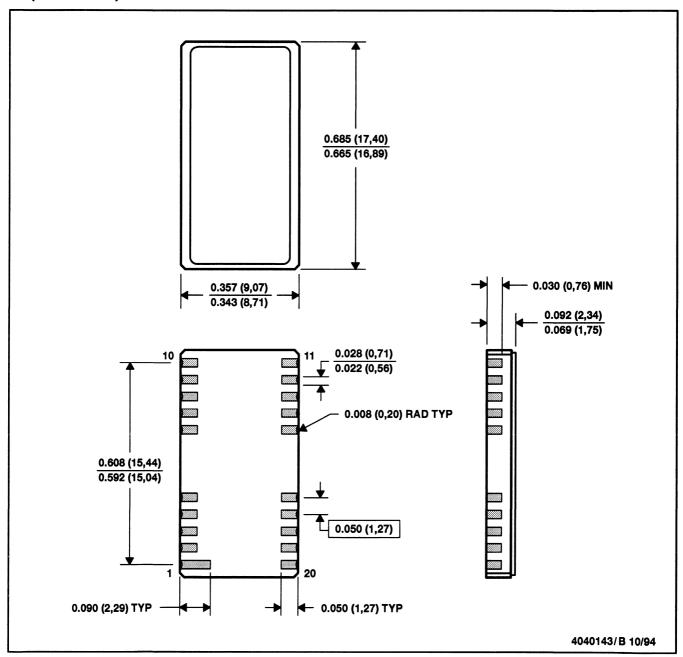


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



FQ (R-CDCC-N20)

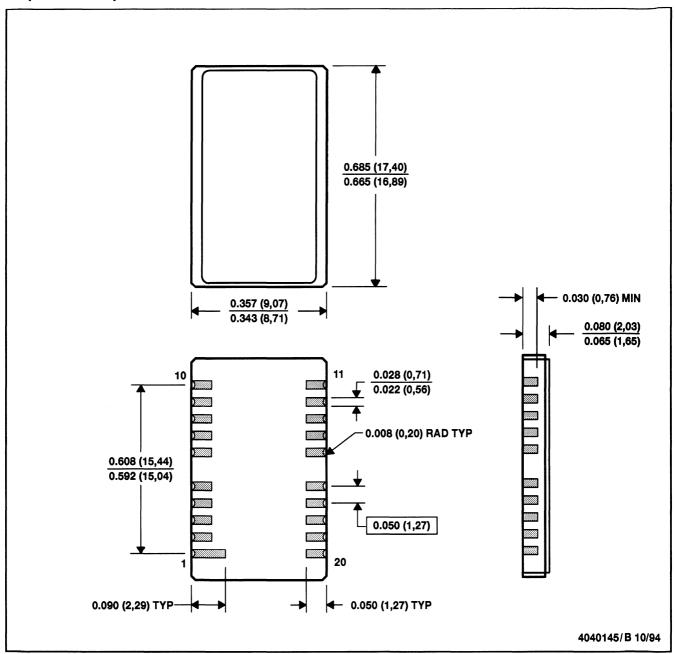
LEADLESS CERAMIC CHIP CARRIER



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

HL (R-CDCC-N20)

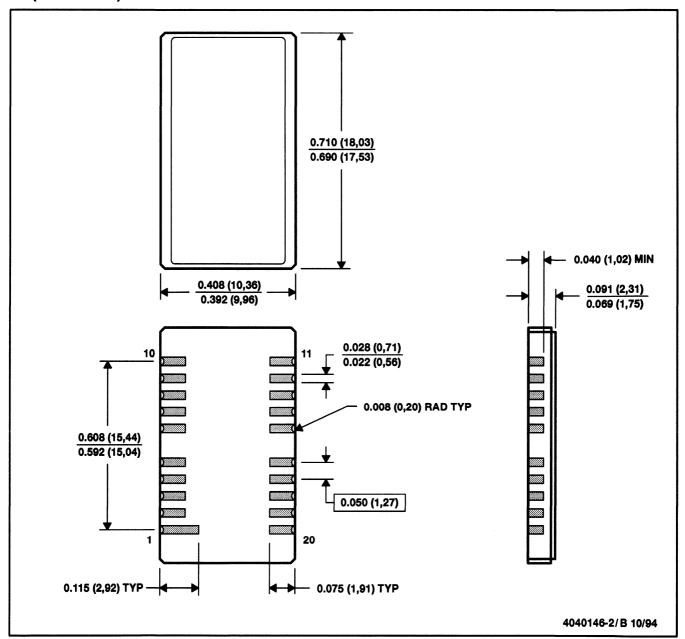
LEADLESS CERAMIC CHIP CARRIER



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

HM (R-CDCC-N20)

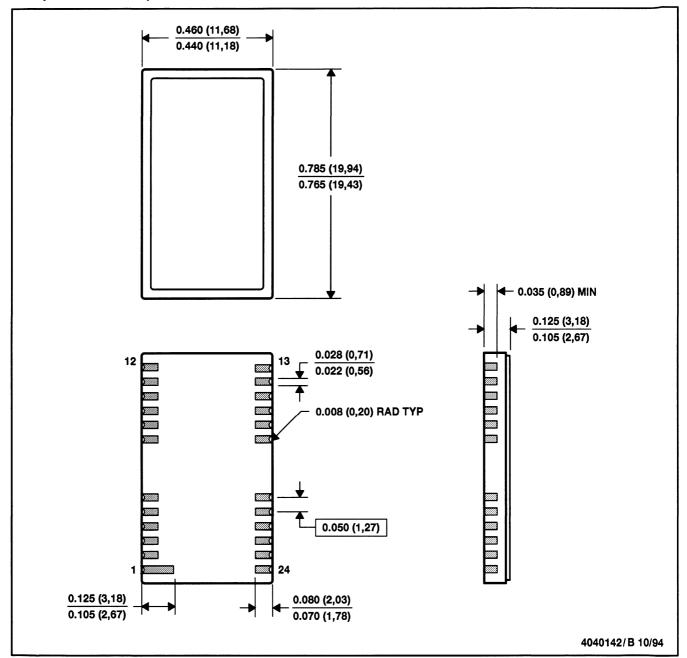
LEADLESS CERAMIC CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.

FNC (R-CDCC-N24/28)

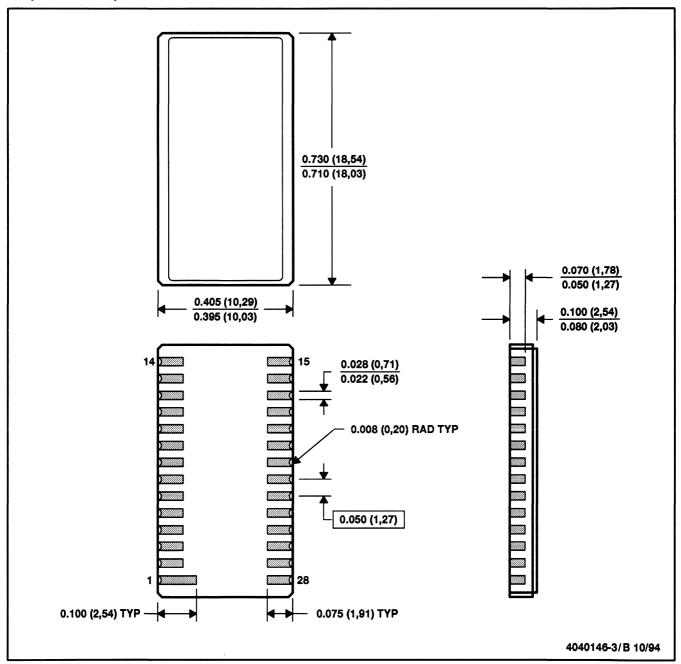
LEADLESS CERAMIC CHIP CARRIER



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

HM (R-CDCC-N28)

LEADLESS CERAMIC CHIP CARRIER



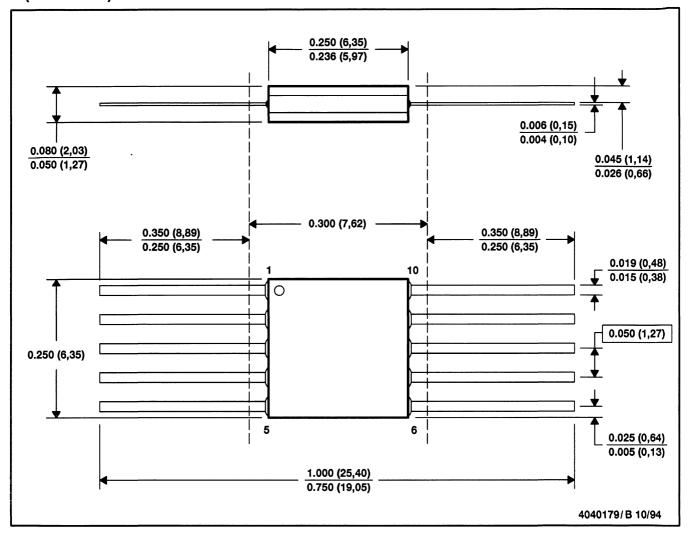
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.



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U (S-GDFP-F10)

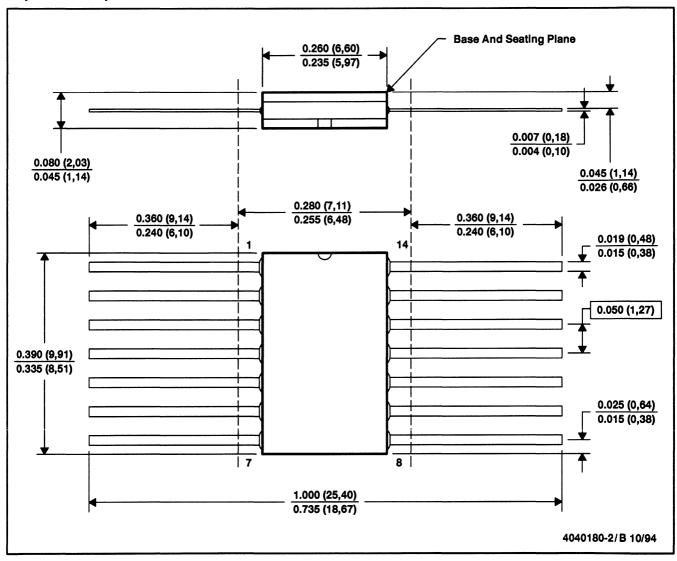
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

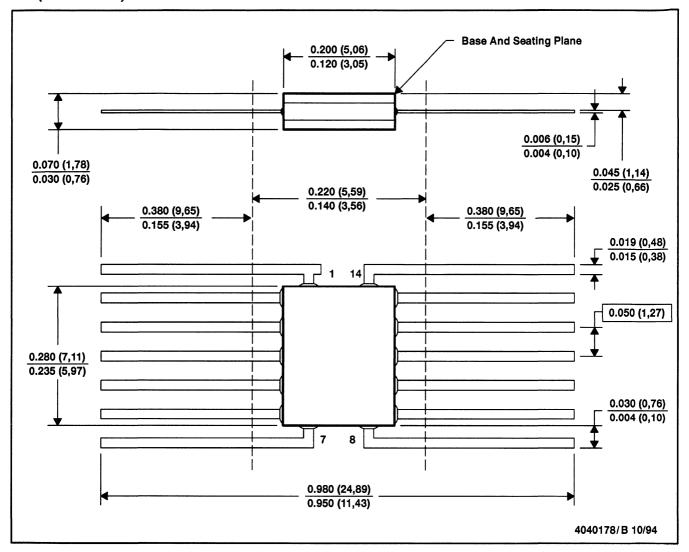


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification onlyE. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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WA (R-GDFP-F14)

CERAMIC DUAL FLATPACK

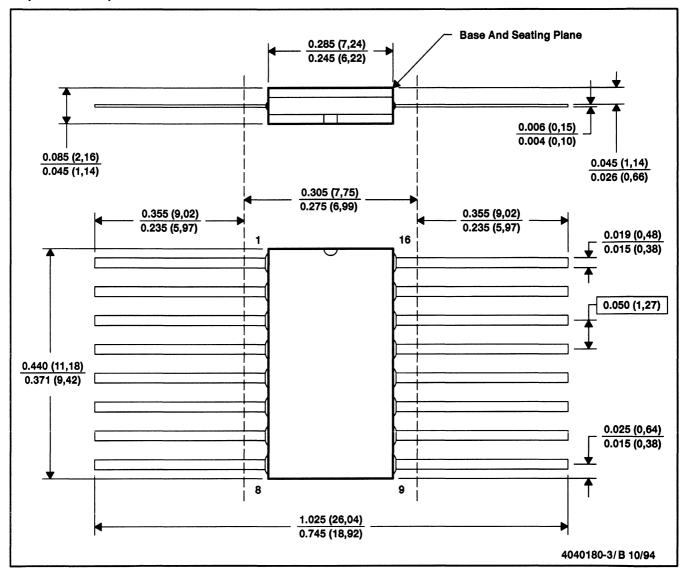


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

W (R-GDFP-F16)

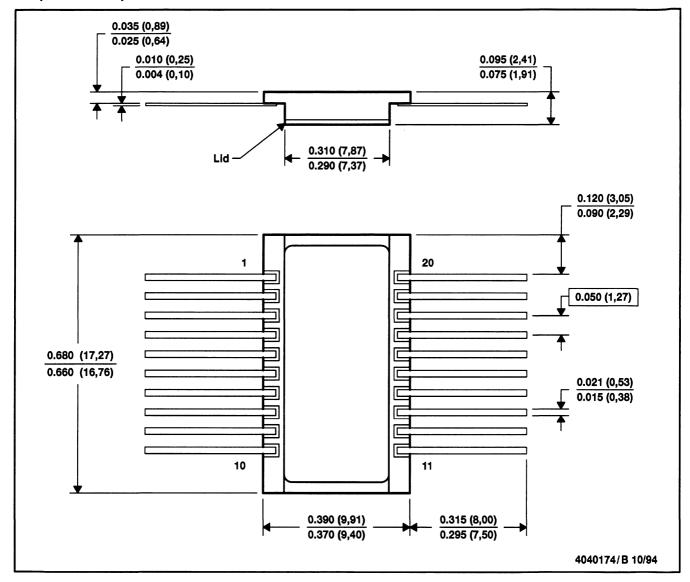
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

HK (R-CDFP-F20)

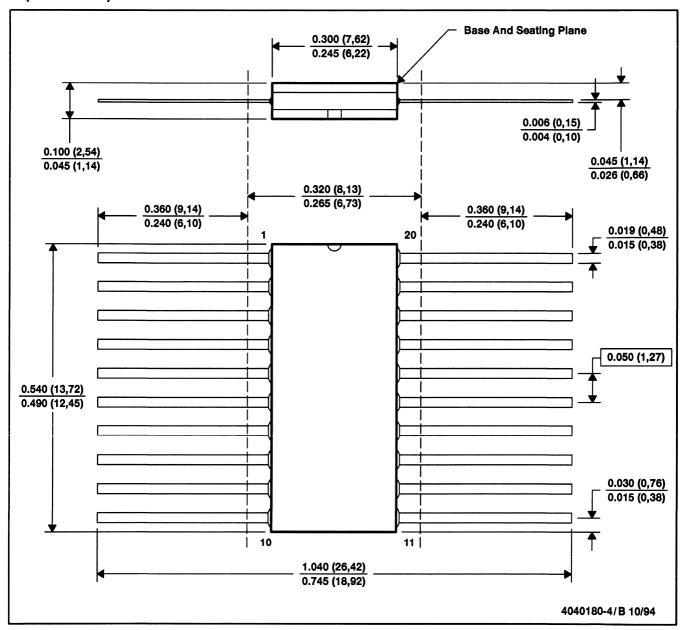
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

W (R-GDFP-F20)

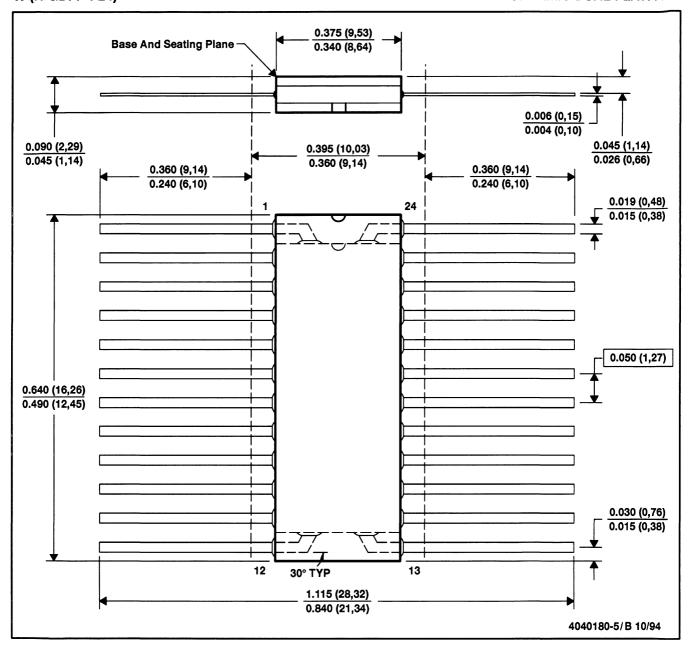
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL-STD-1835 GDFP2-F20

W (R-GDFP-F24)

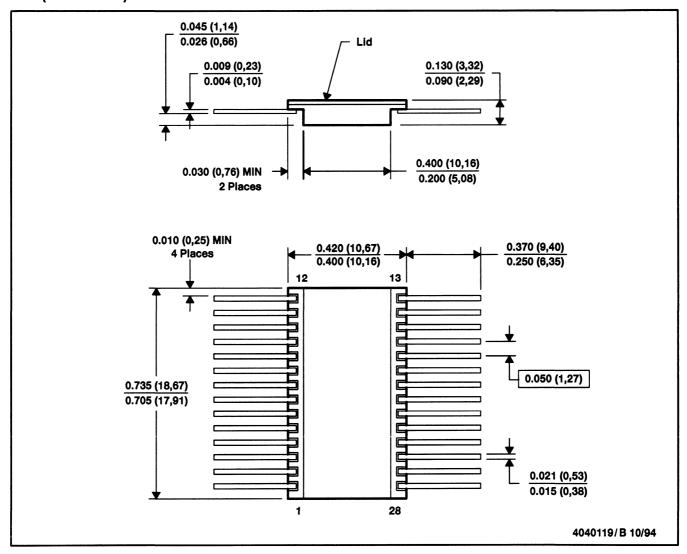
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
- E. Index point is provided on cap for terminal identification only

HKA (R-CDFP-F28)

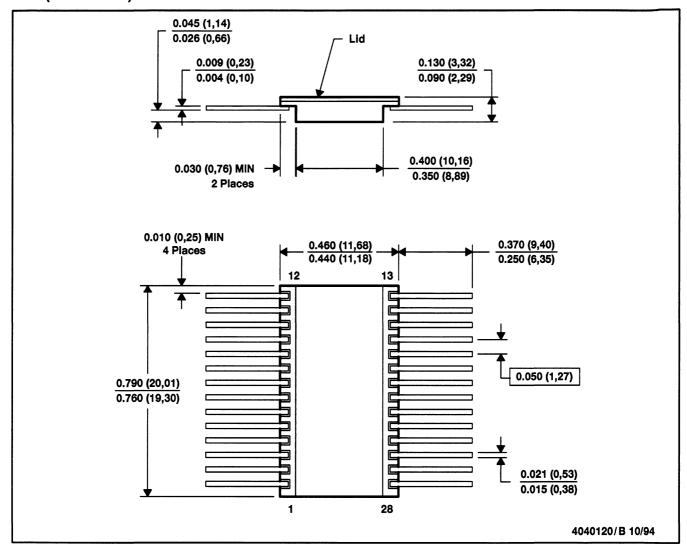
CERAMIC DUAL FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

HKB (R-CDFP-F28)

CERAMIC DUAL FLATPACK

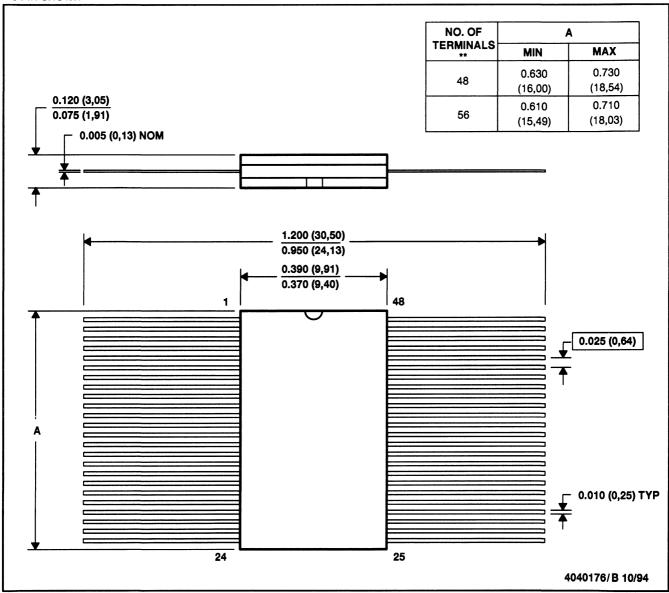


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 PIN SHOWN

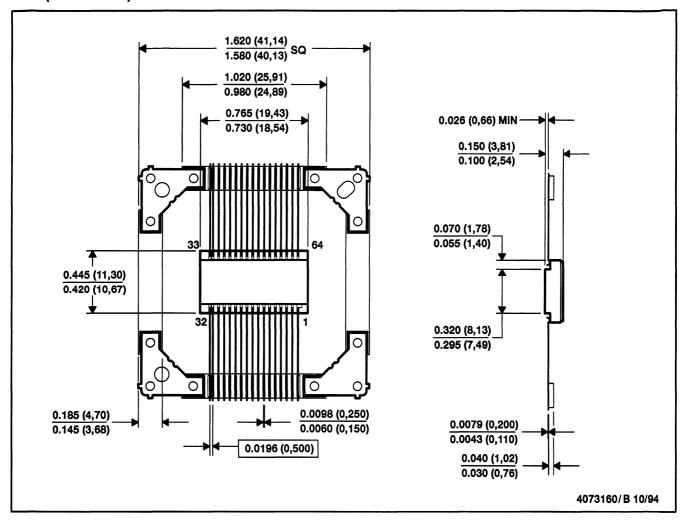


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA GDFP1-F56 and JEDEC MO-146AB



HKC (R-CDFP-F64)

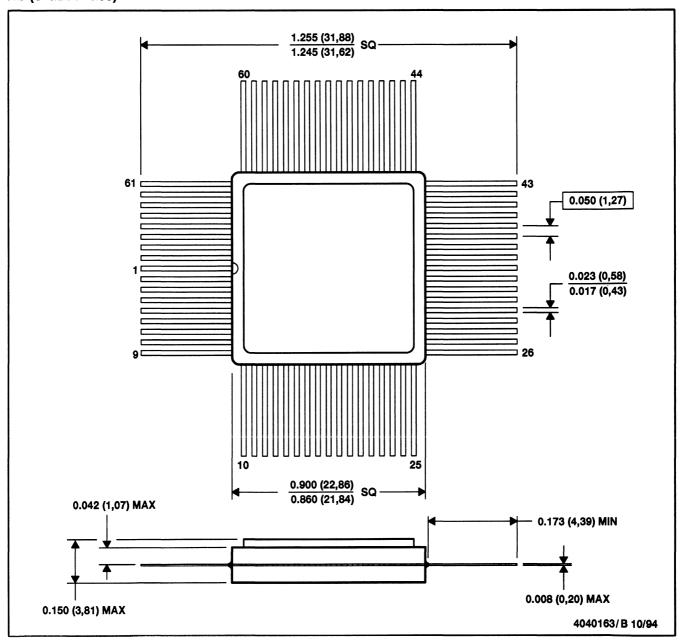
CERAMIC DUAL FLATPACK WITH TIE BAR



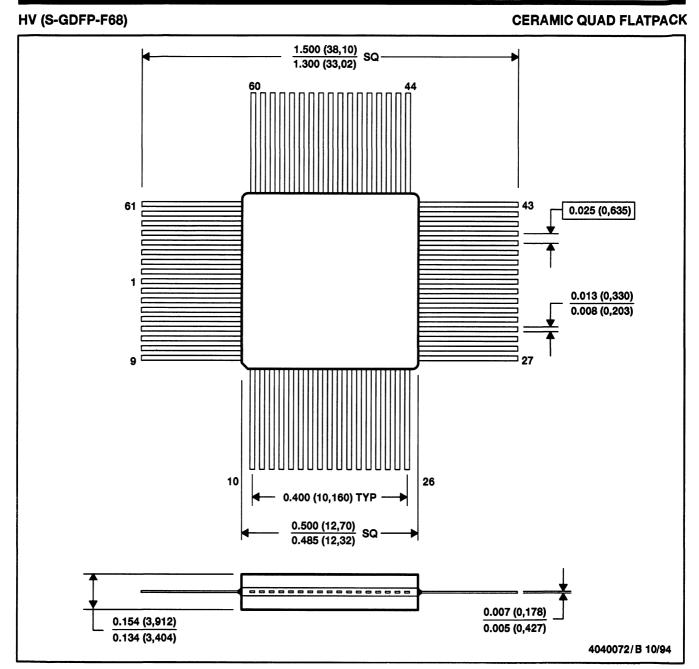
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. All leads not shown for clarity purposes.

HB (S-GDFP-G68)

CERAMIC QUAD FLATPACK



- B. This drawing is subject to change without notice.C. This package can be hermetically sealed with a metal lid.

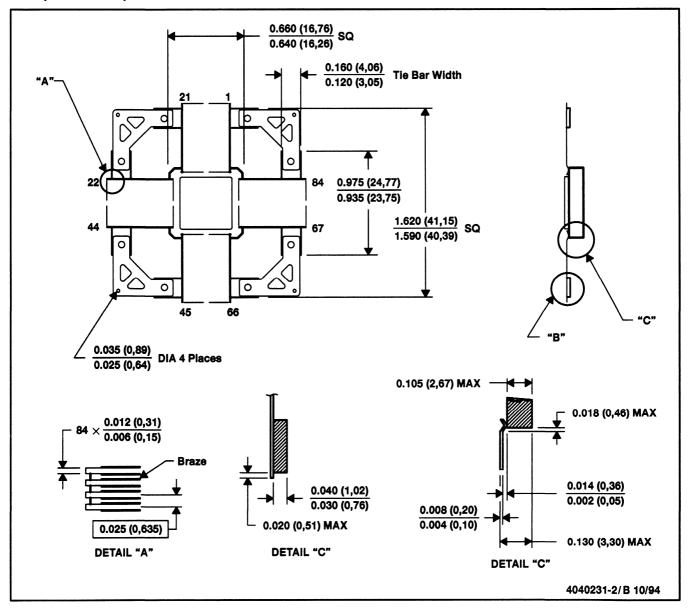


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

HFG (S-CQFP-F84)

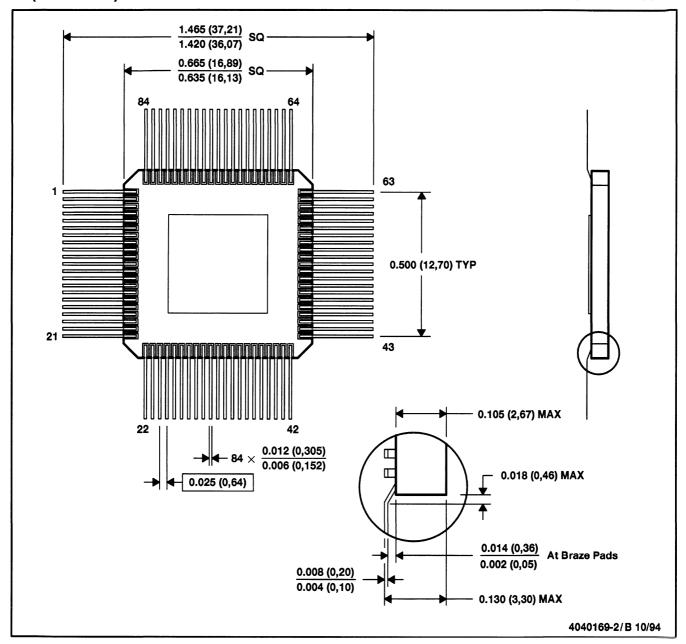
CERAMIC QUAD FLATPACK WITH TIE BAR



- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to nonconductive tie bar carrier
- D. This package can be hermetically sealed with a metal lid.
- E. The terminals are gold plated.

HT (S-CQFP-F84)

CERAMIC QUAD FLATPACK

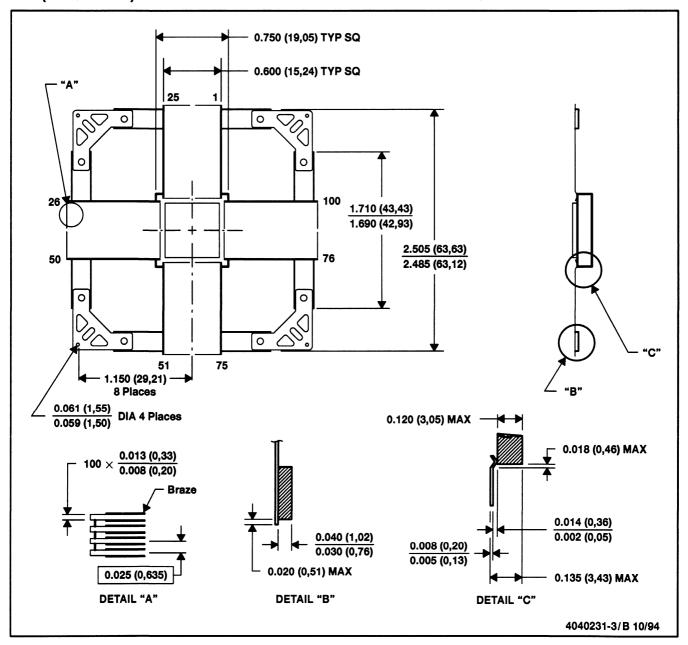


- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.

 E. Falls within JEDEC MO-090 AA

HFG (S-CQFP-F100)

CERAMIC QUAD FLATPACK WITH TIE BAR

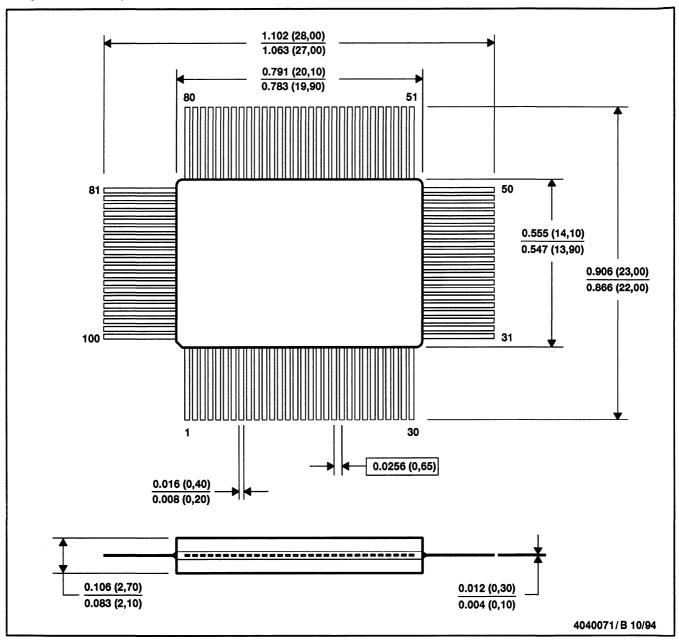


- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
- D. This package can be hermetically sealed with a metal lid.
- E. The terminals are gold plated.
- F. Falls within JEDEC MO-113 AD





CERAMIC QUAD FLATPACK

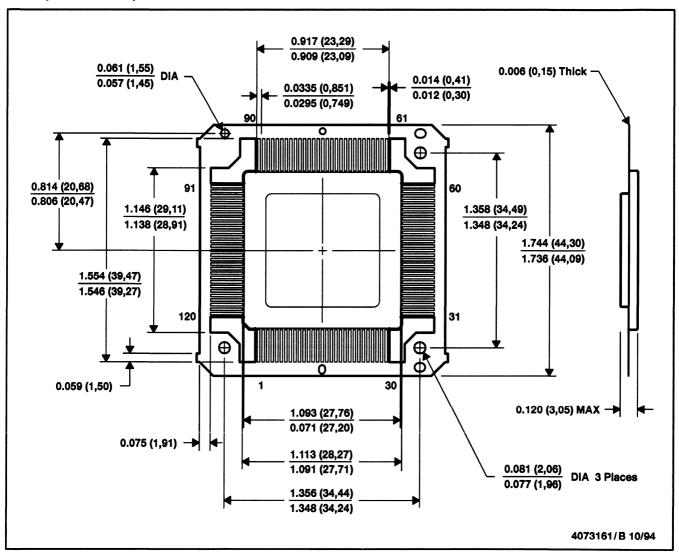


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

HBG (S-CQFP-F120)

CERAMIC FLATPACK WITH TIE-BAR CARRIER

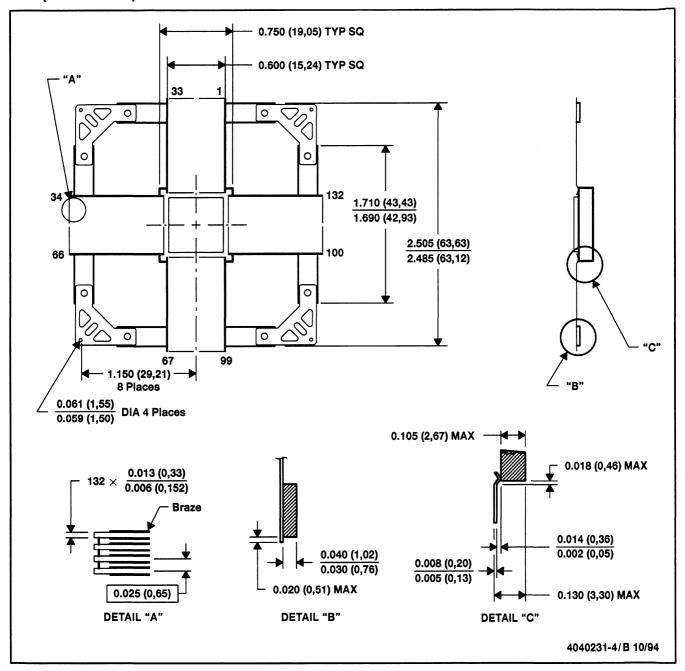


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

HFG (S-CQFP-F132)

CERAMIC QUAD FLATPACK WITH TIE BAR

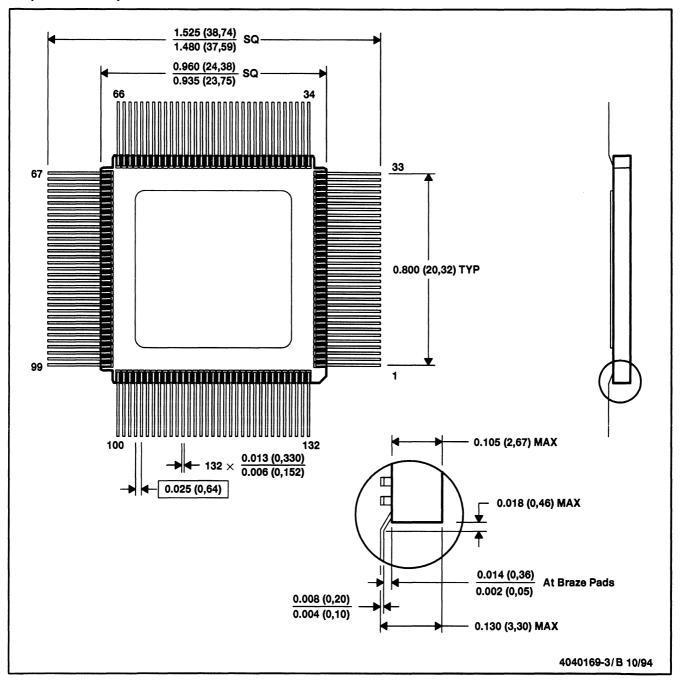


- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
- D. This package can be hermetically sealed with a metal lid.
- E. The terminals are gold plated.
- F. Falls within JEDEC MO-113 AC



HT (S-CQFP-F132)

CERAMIC QUAD FLATPACK

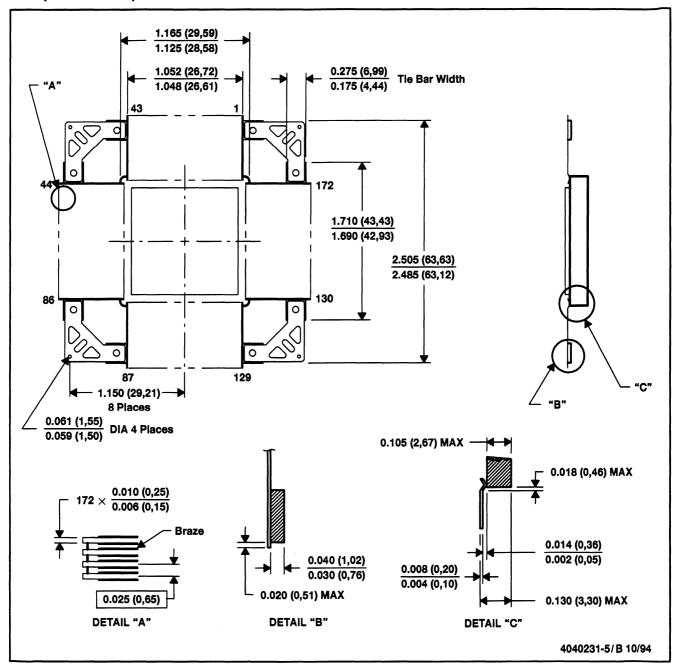


- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-090 AB



HFG (S-CQFP-F172)

CERAMIC QUAD FLATPACK WITH TIE BAR

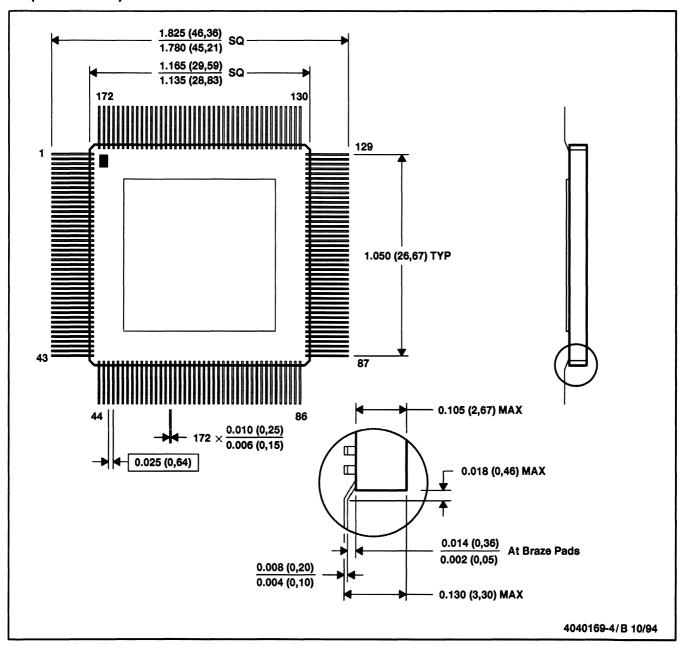


- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
 - D. This package can be hermetically sealed with a metal lid.
 - E. The terminals are gold plated.
 - F. Falls within JEDEC MO-113 AE



HT (S-CQFP-F172)

CERAMIC QUAD FLATPACK

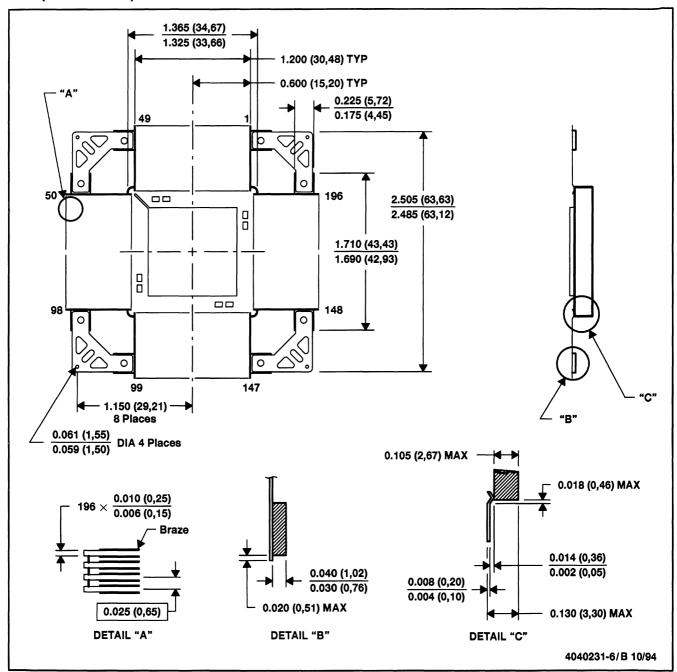


- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-090 AD



HFG (S-CQFP-F196)

CERAMIC QUAD FLATPACK WITH TIE BAR

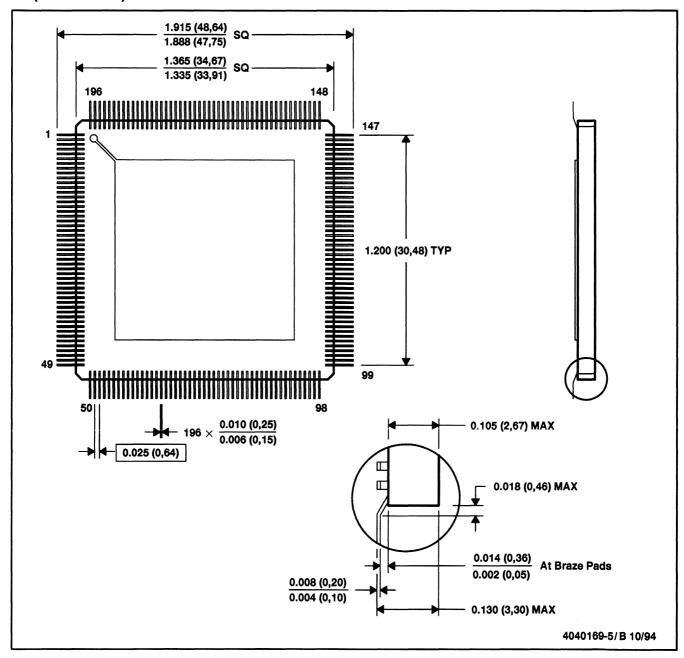


- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
- D. This package can be hermetically sealed with a metal lid.
- E. The terminals are gold plated.
- F. Falls within JEDEC MO-113 AB



HT (S-CQFP-F196)

CERAMIC QUAD FLATPACK



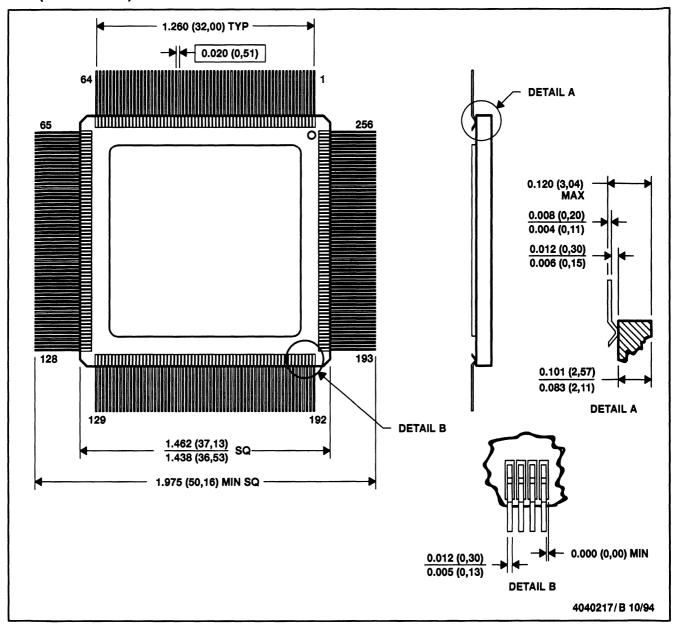
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-090 AE



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HFA (S-CQFP-F256)

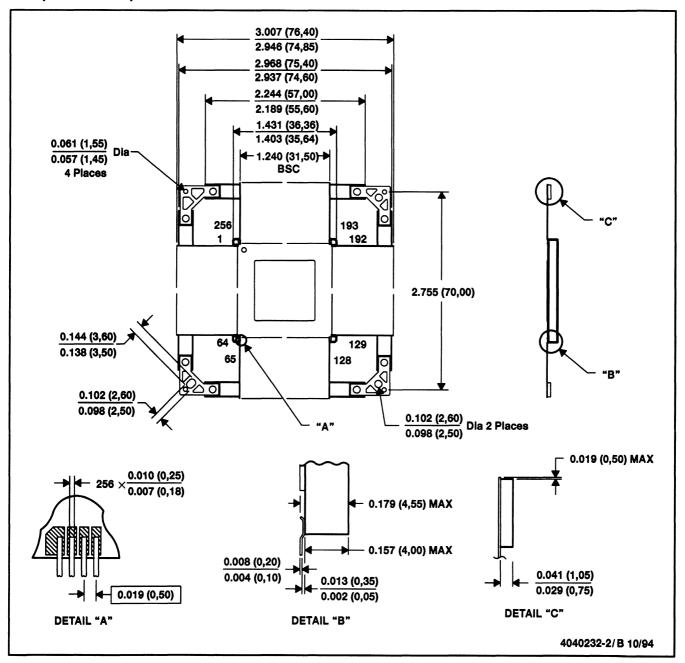
CERAMIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.

HFH (R-CQFP-F256)

CERAMIC QUAD FLATPACK WITH TIE BAR

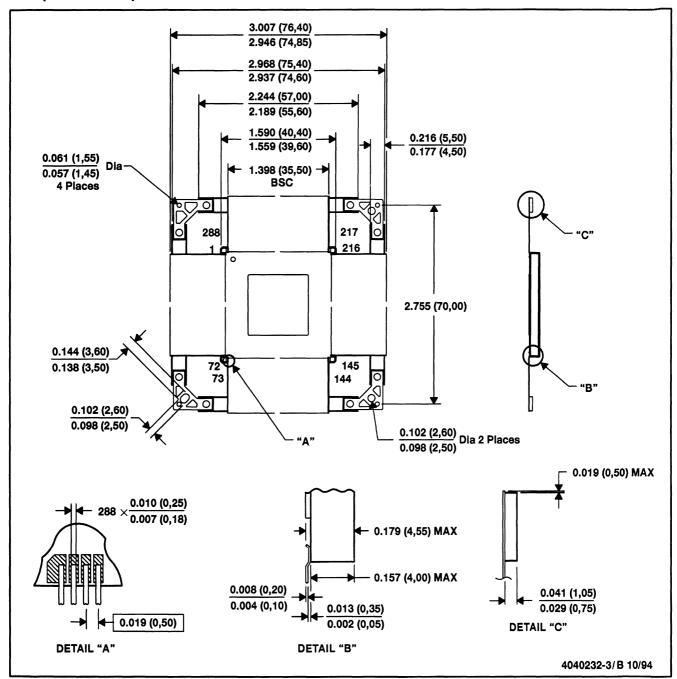


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-134 AB



HFH (R-CQFP-F288)

CERAMIC QUAD FLATPACK WITH TIE BAR

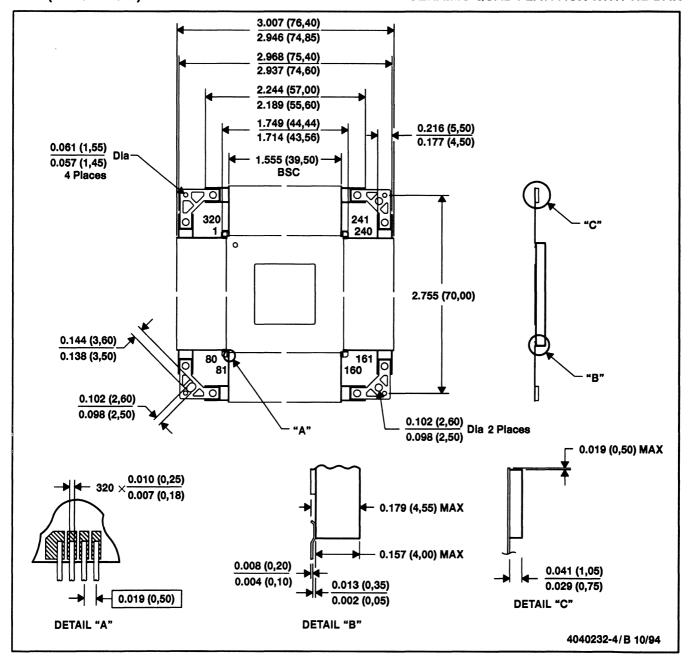


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-134 AC



HFH (R-CQFP-F320)

CERAMIC QUAD FLATPACK WITH TIE BAR

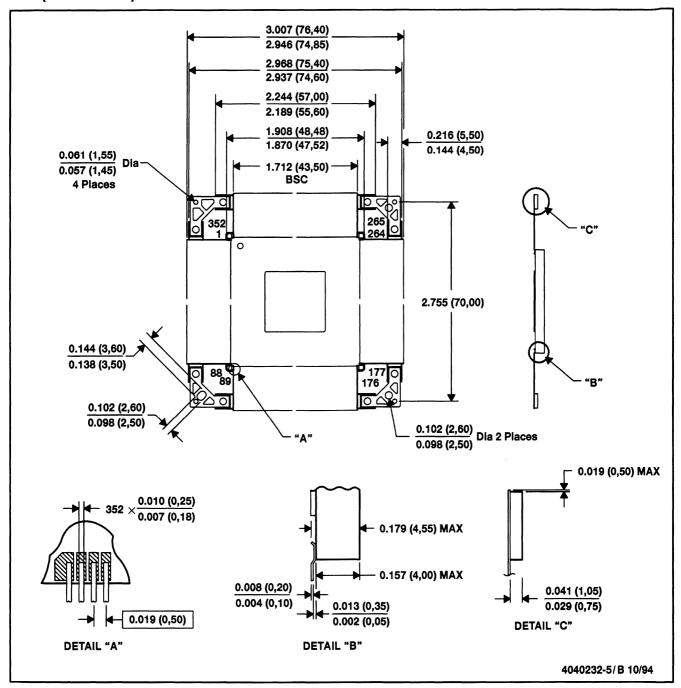


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-134 AD



HFH (S-CQFP-F352)

CERAMIC QUAD FLATPACK WITH TIE BAR

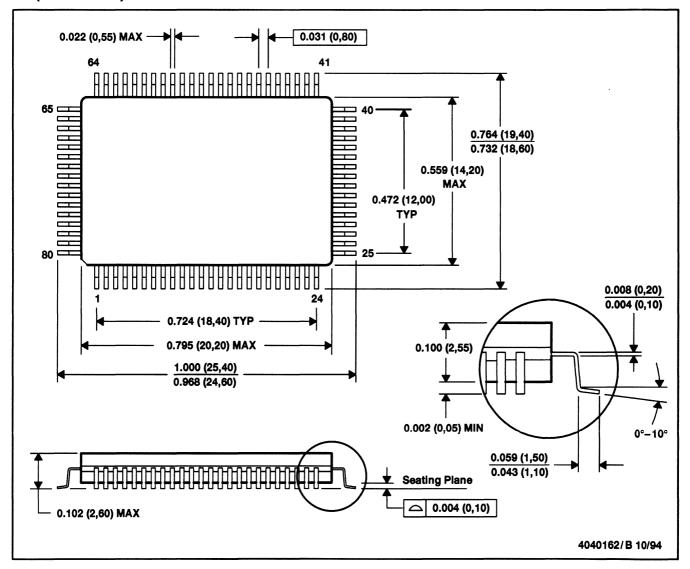


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MO-134 AE



HD (R-GQFP-G80)

CERAMIC QUAD FLATPACK

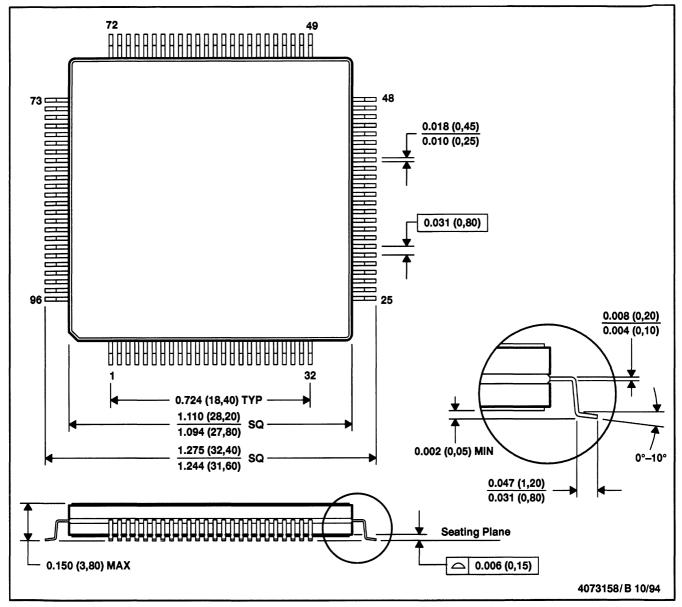


NOTES: A. All linear dimensions are in inches (millimeters).

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HH (S-GQFP-G96)

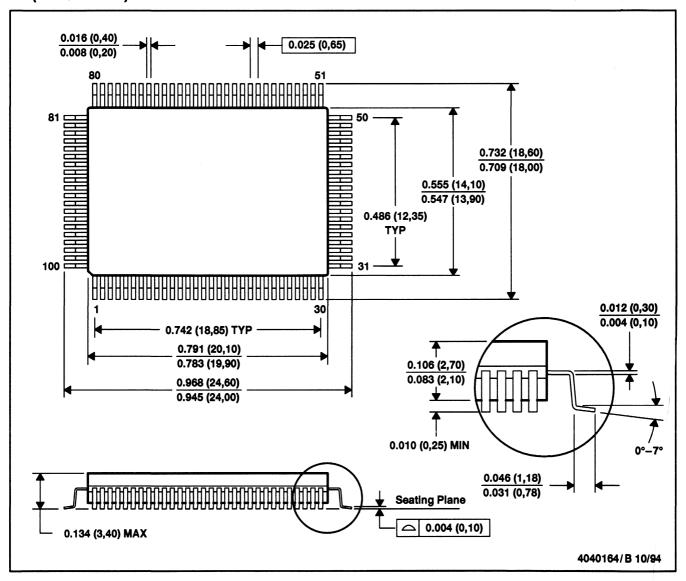
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).

HE (R-GQFP-G100)

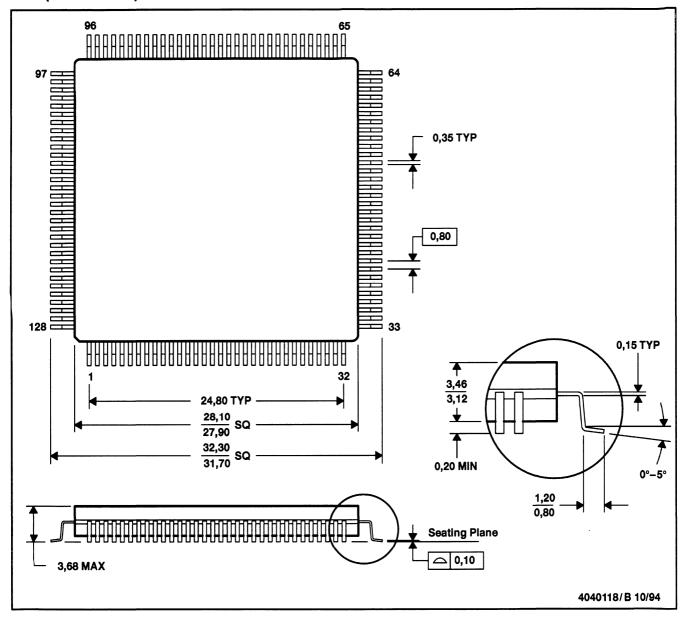
CERAMIC QUAD FLATPACK



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

HGA (S-CQFP-F128)

CERAMIC QUAD FLATPACK

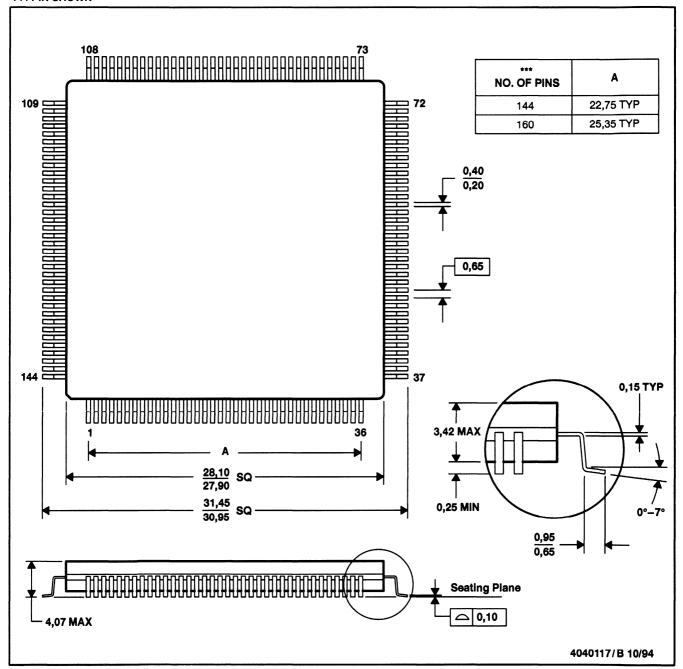


NOTES: A. All linear dimensions are in millimeters.

HP (S-GQFP-G***)

CERAMIC QUAD FLATPACK

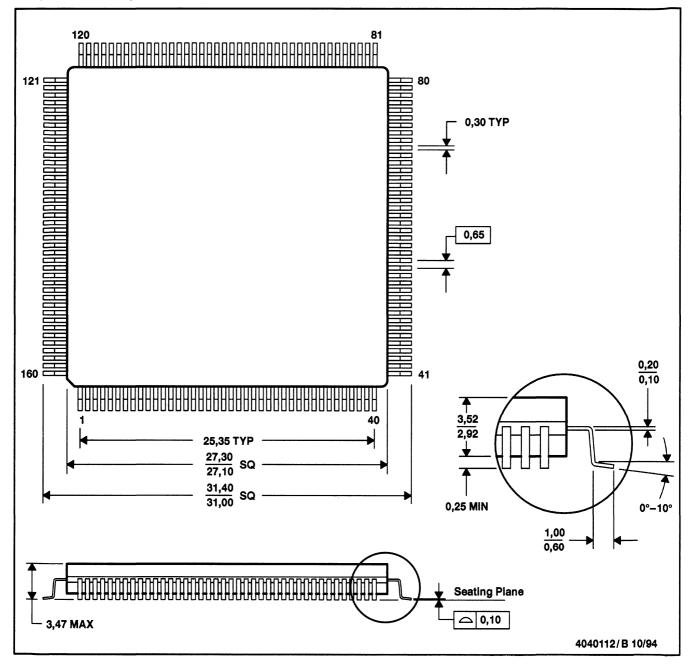
144 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

HY (S-CQFP-G160)

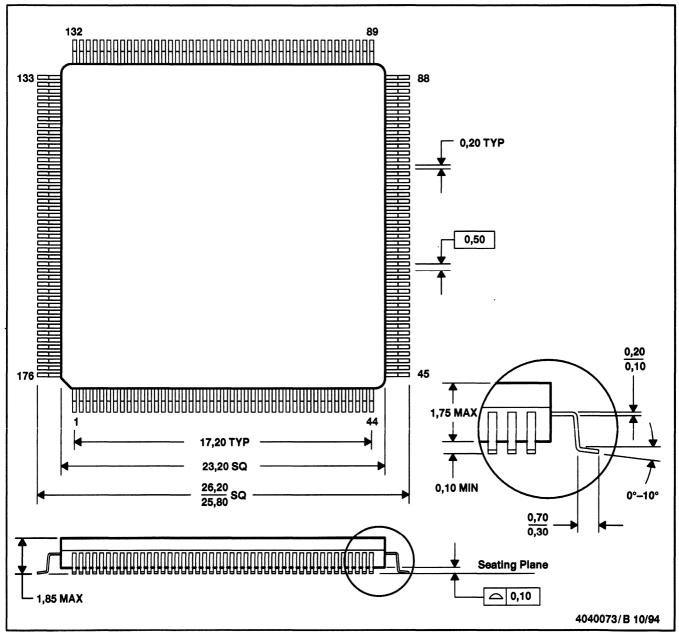
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

HZ (S-CQFP-G176)

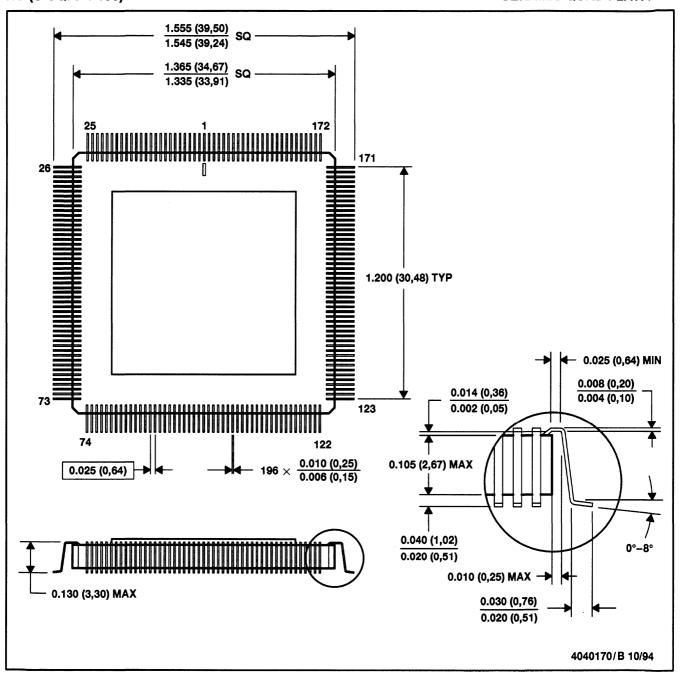
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

HU (S-CQFP-F196)

CERAMIC QUAD FLATPACK

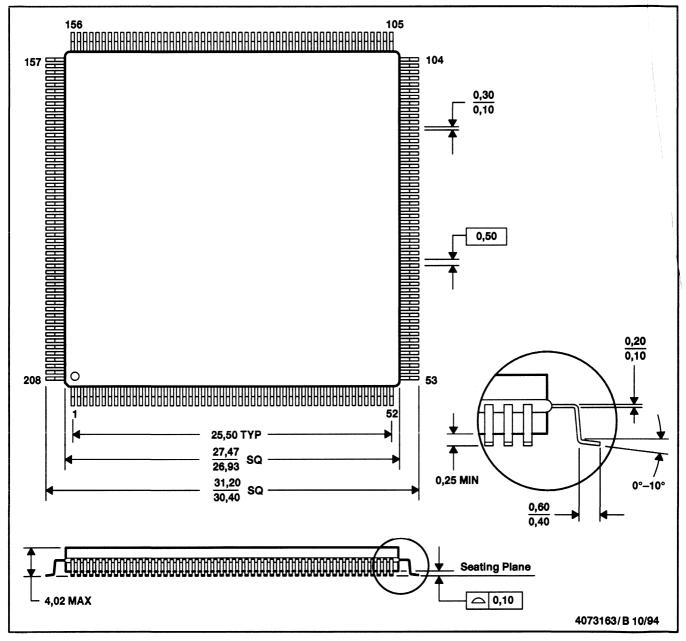


- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.



HAF (S-GQFP-G208)

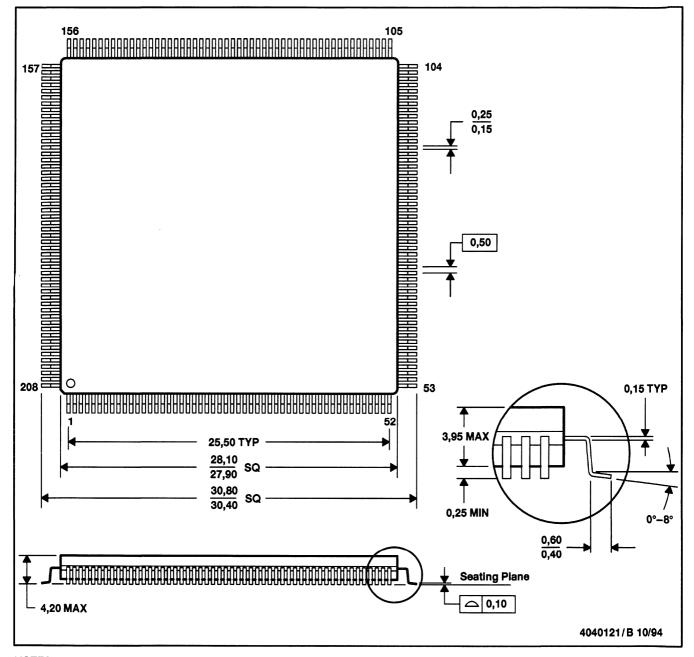
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

HPA (S-GQFP-G208)

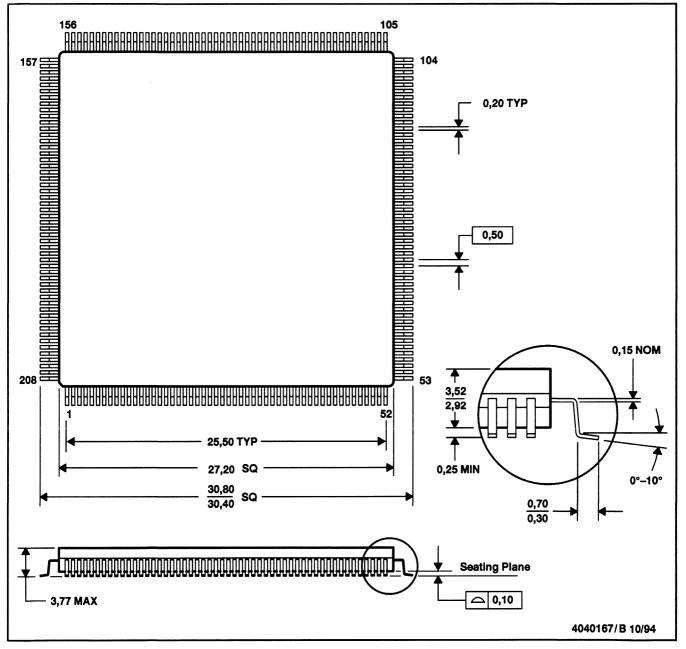
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

WF (S-GQFP-G208)

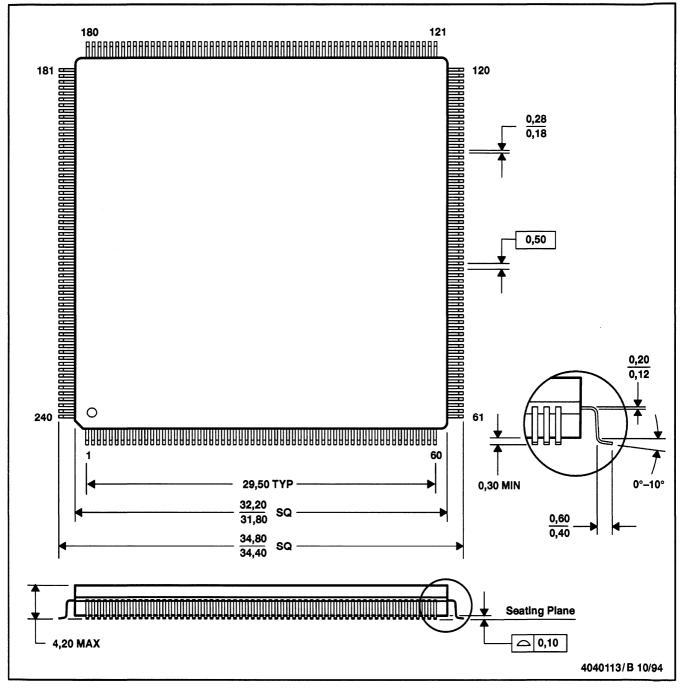
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

HPC (S-GQFP-G240)

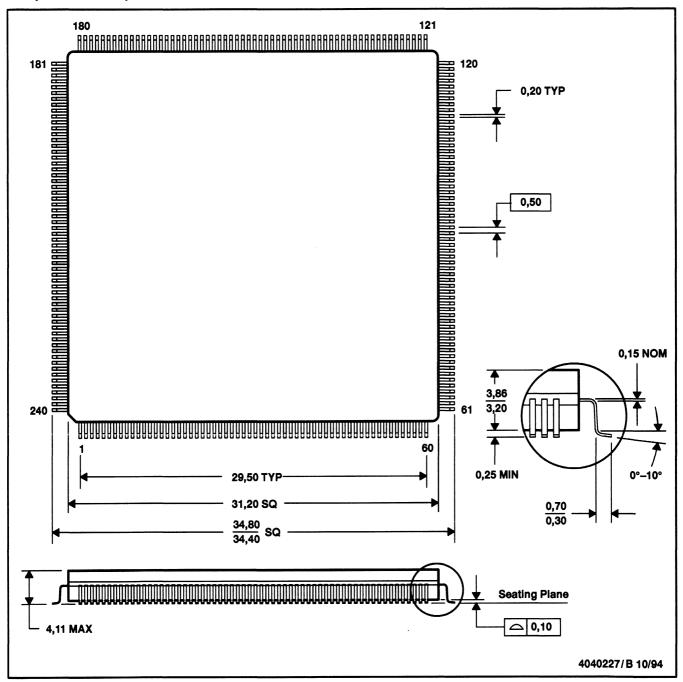
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

WG (S-GQFP-G240)

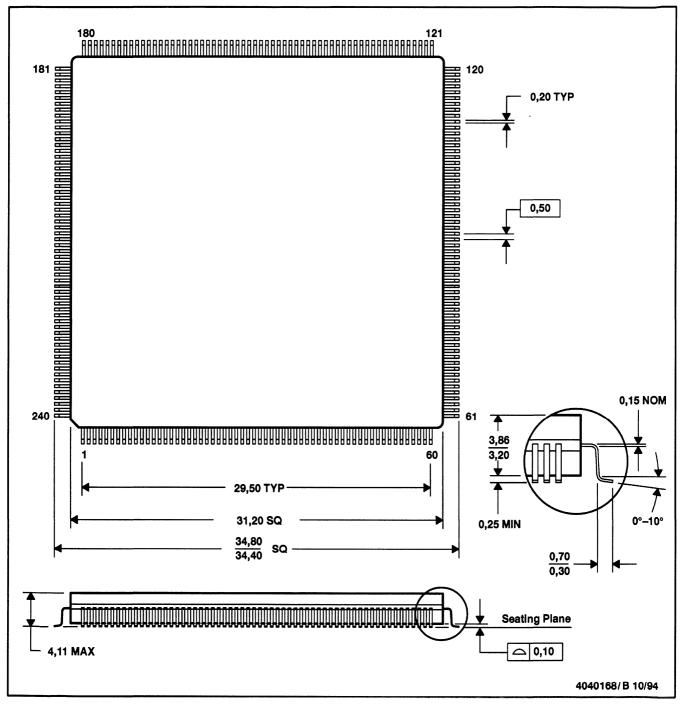
CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

WH (S-GQFP-G240)

CERAMIC QUAD FLATPACK



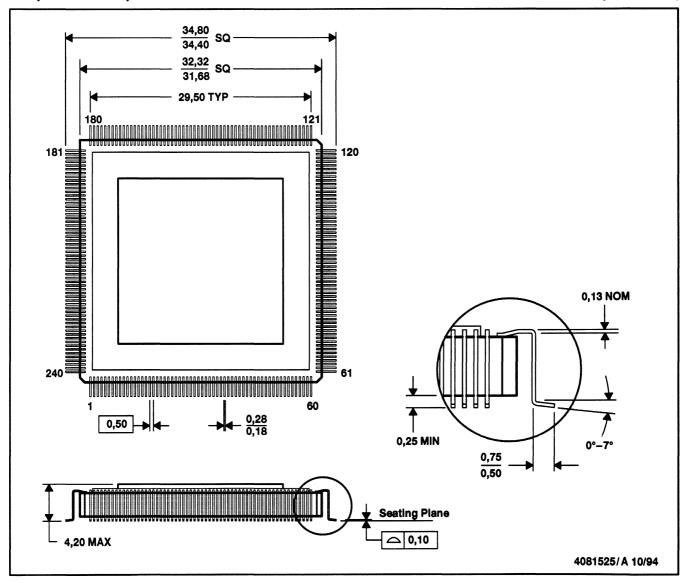
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Ceramic material is ALN.

WK (S-CQFP-G240)

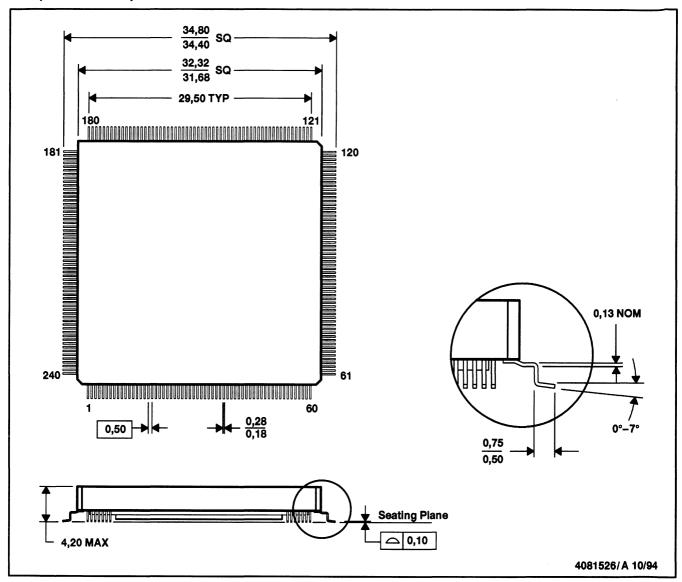
CERAMIC QUAD FLATPACK (CAVITY-UP)



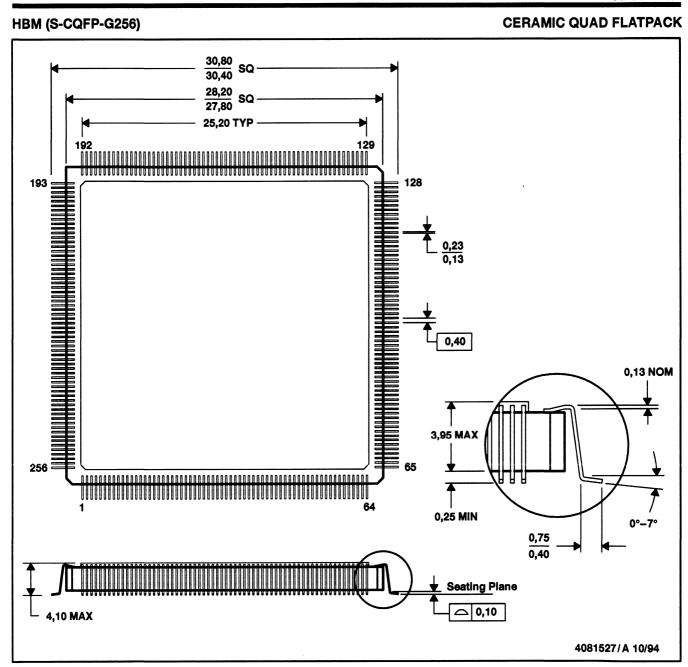
NOTES: A. All linear dimensions are in millimeters.



CERAMIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.



NOTES: A. All linear dimensions are in millimeters.

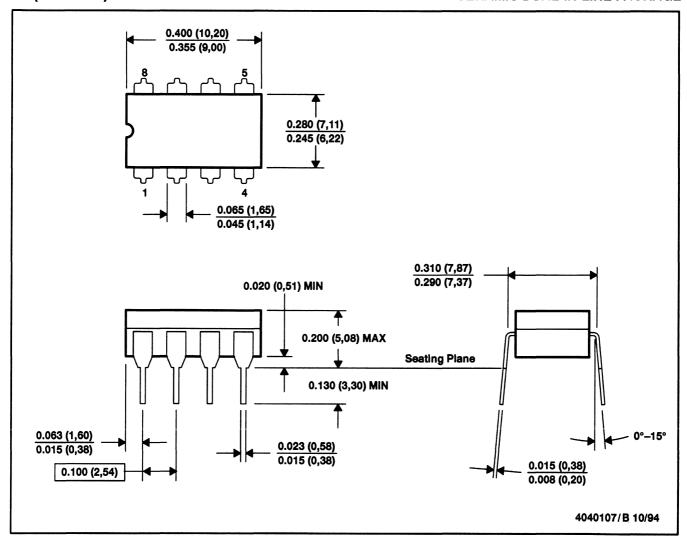
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CDIP SB (SIDE-BRAZE CERAMIC DUAL-IN-LINE PACKAGE)	16/18/20/24 18/20	300 MIL	JD JDB	4040086 4040090	5–11 5–12
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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



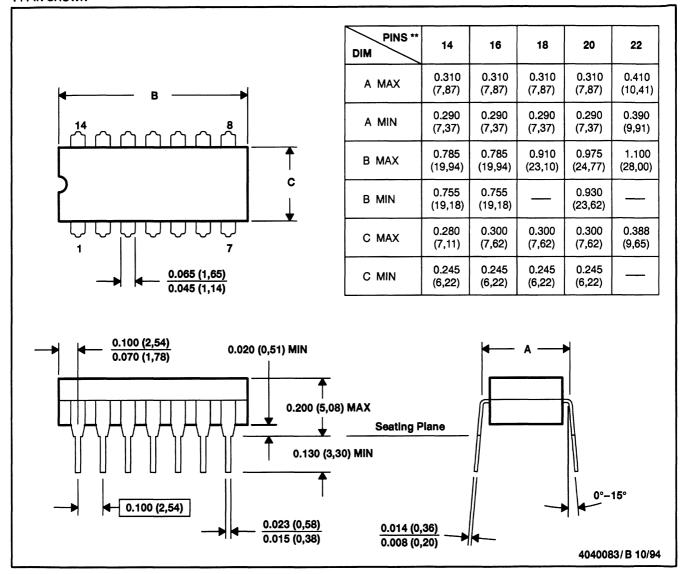
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T8

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

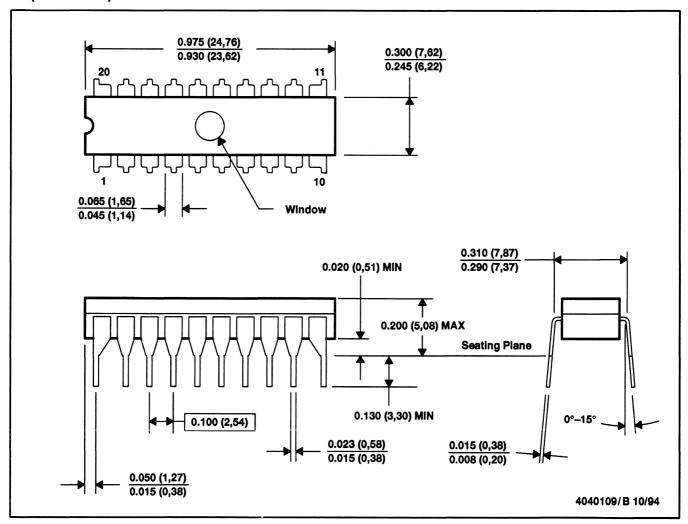
14 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

JL (R-GDIP-T20)

CERAMIC DUAL-IN-LINE PACKAGE



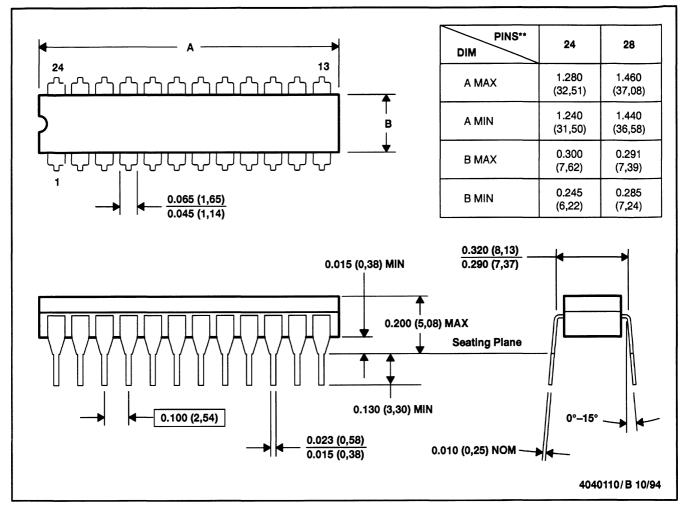
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T20

OCTOBER 1994

JT (R-GDIP-T**)

24 PIN SHOWN

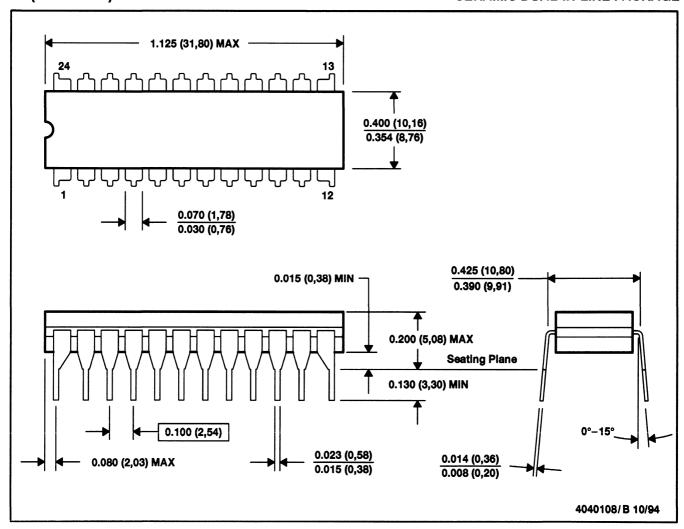
CERAMIC DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB

JK (R-GDIP-T24)

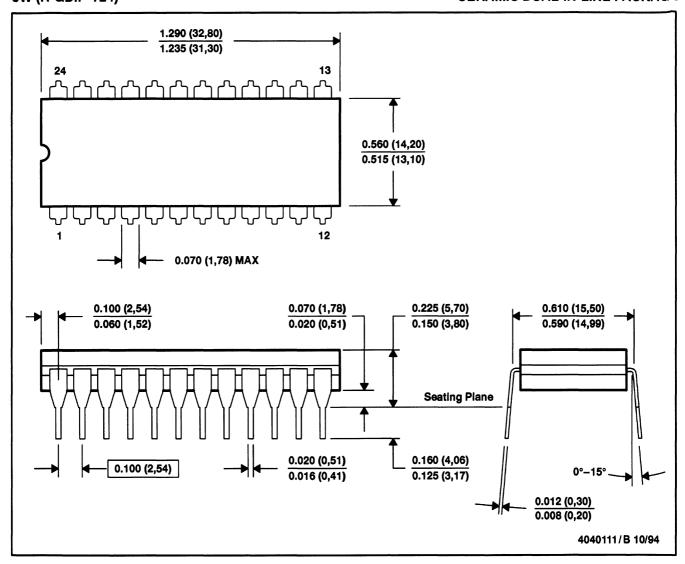
CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
 - E. Falls within MIL-STD-1835 GDIP5-T24

JW (R-GDIP-T24)

CERAMIC DUAL-IN-LINE PACKAGE

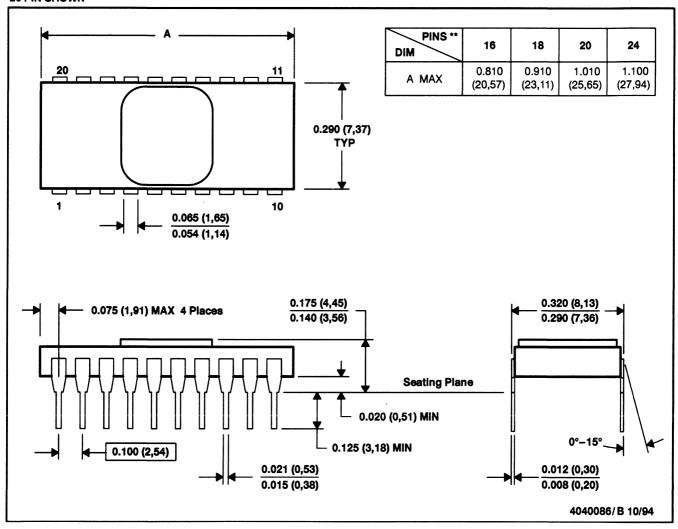


- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
 - E. Falls within MIL-STD-1835 GDIP5-T24

JD (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PIN SHOWN

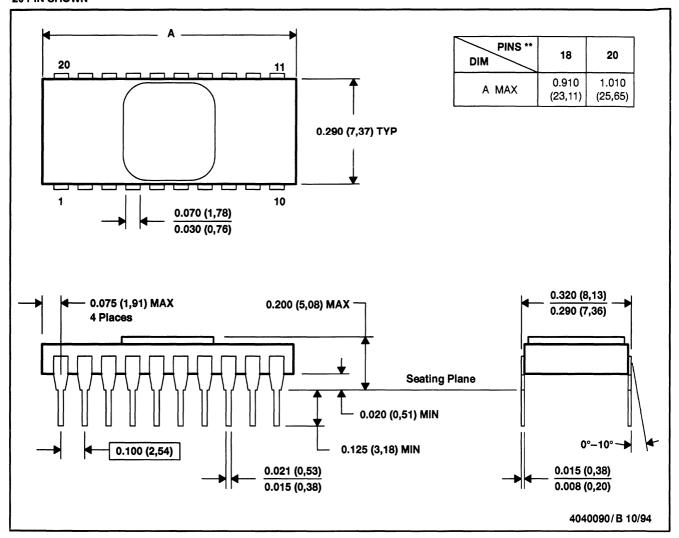


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

JDB (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

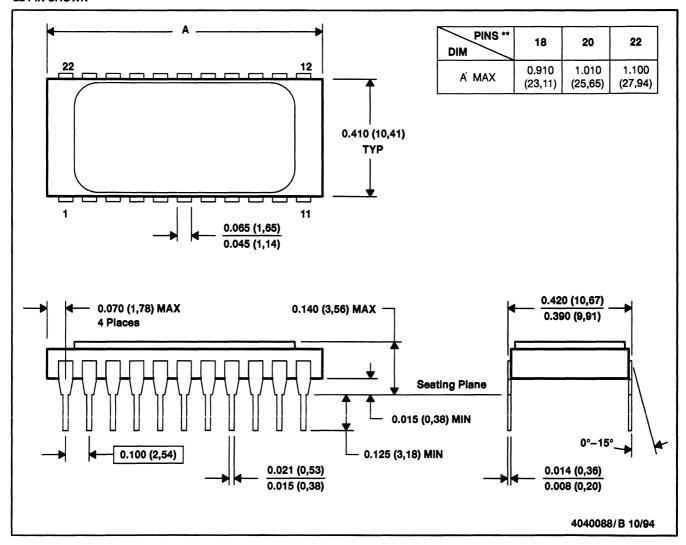
B. This drawing is subject to change without notice.

C. Falls within MIL-STD-1835 GDIP1-T18, GDIP1-T20 and JEDEC MS-015 AD, MS-015 AE

JD(R-CDIP-T**)

22 PIN SHOWN

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

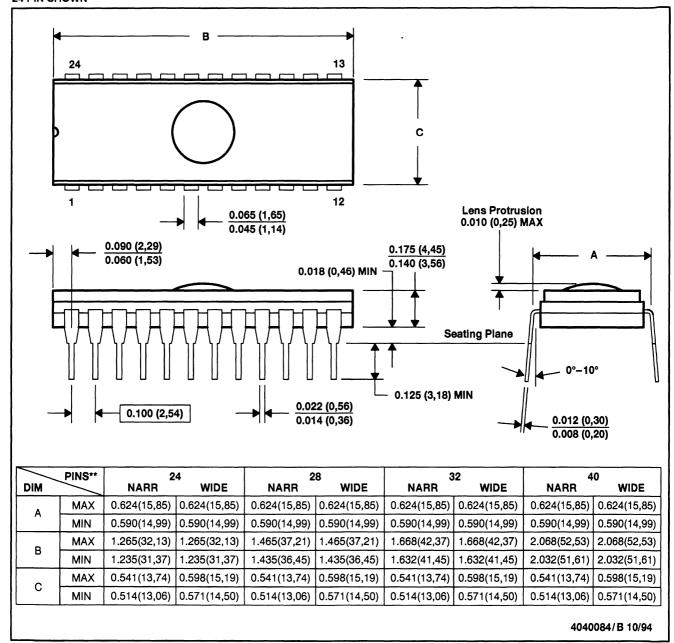


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

J (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

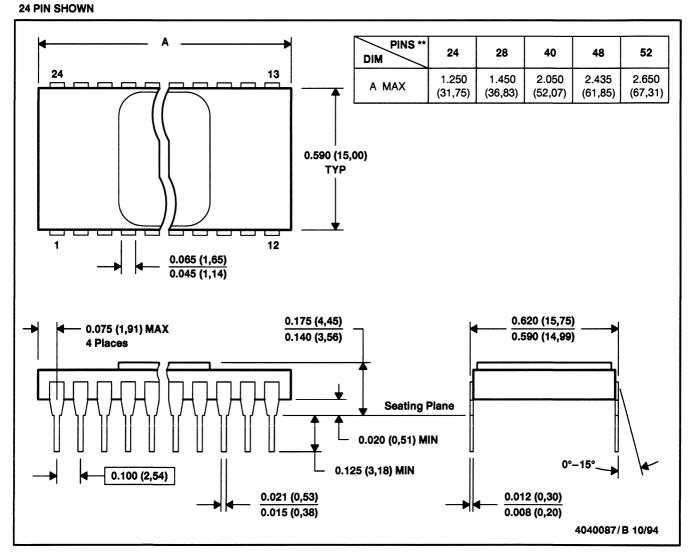
24 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only

JD (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

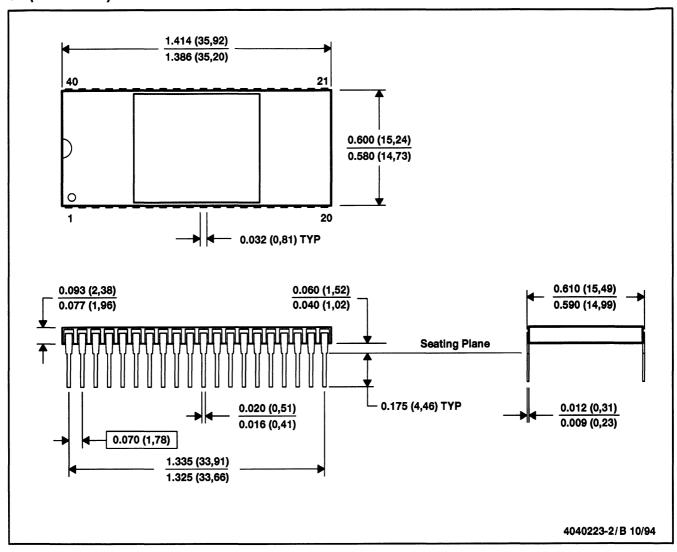


- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

OCTOBER 1994

JC (R-CDIP-T40)

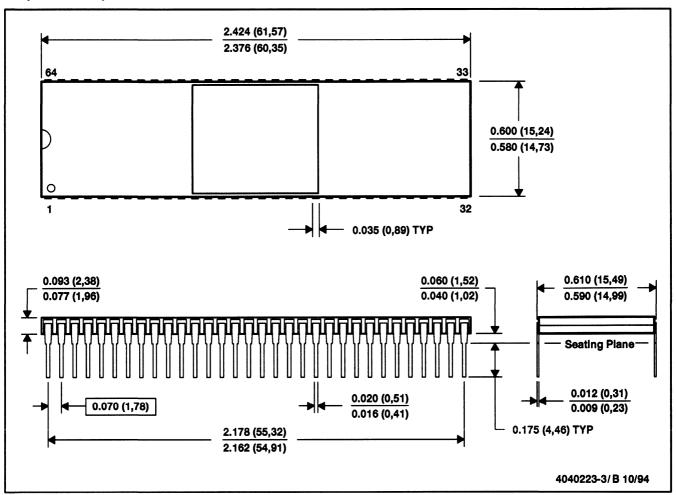
CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

JC (R-CDIP-T64)

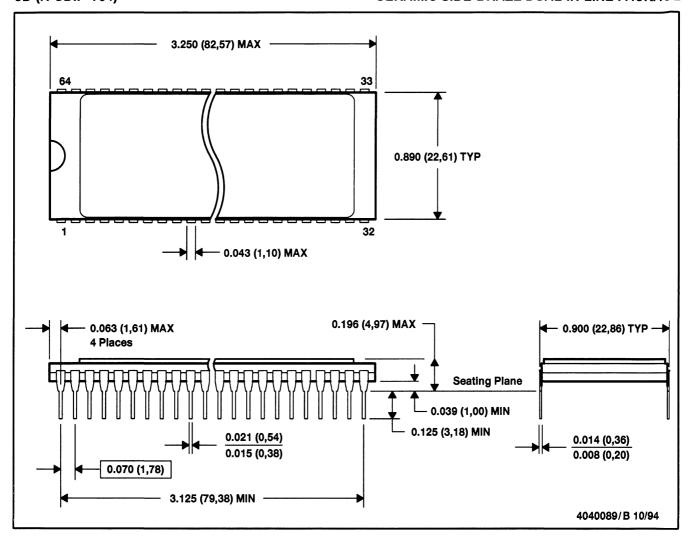
CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.

JD (R-CDIP-T64)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE



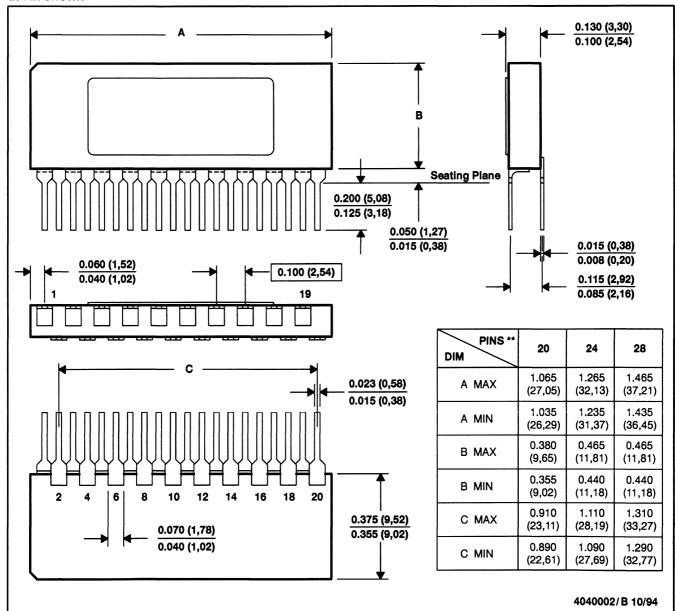
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

SV (R-CZIP-T**)

CERAMIC ZIG-ZAG PACKAGE

20 PIN SHOWN

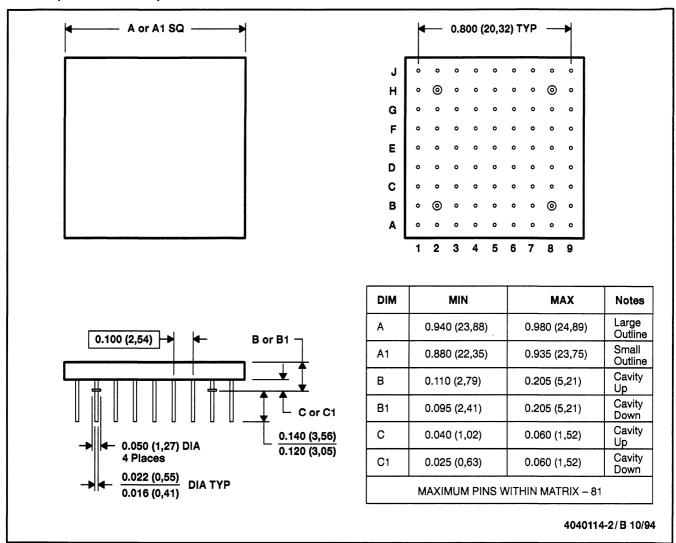


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

GA-GB (S-CPGA-P9 X 9)

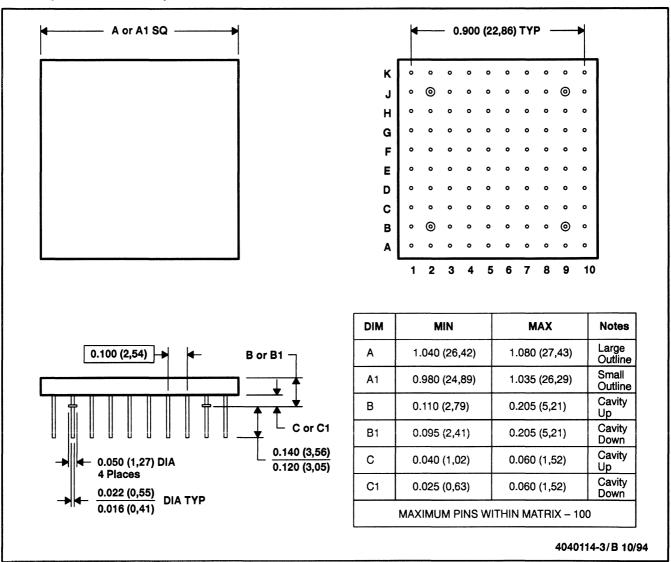
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA1-PN and CMGA13-PN and JEDEC MO-067AA and MO-066AA, respectively

GA-GB (S-CPGA-P10 X 10)

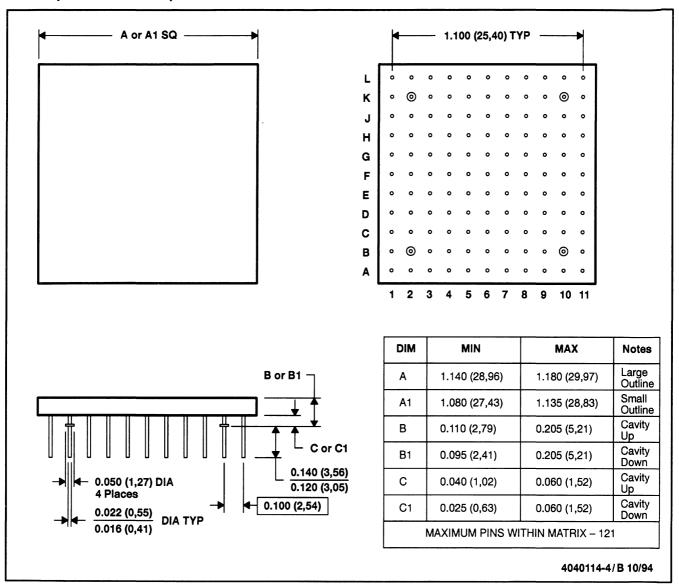
CERAMIC PIN GRID ARRAY PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark may appear on top or bottom depending on package vendor.
 - D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold plated or solder dipped.
 - G. Falls within MIL-STD-1835 CMGA2-PN and CMGA12-PN and JEDEC MO-067AB and MO-066AB, respectively

GA-GB (S-CPGA-P11 X 11)

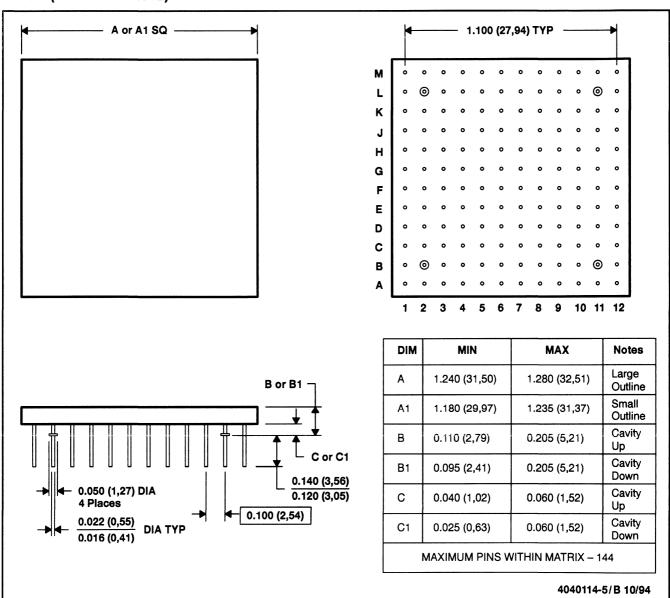
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA3-PN and CMGA15-PN and JEDEC MO-067AC and MO-066AC, respectively

GA-GB (S-CPGA-P12 X 12)

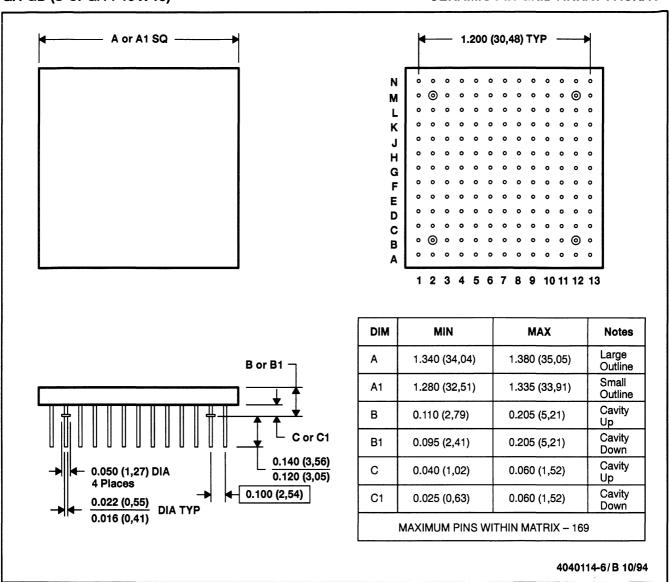
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA4-PN and CMGA16-PN and JEDEC MO-067AD and MO-066AD, respectively

GA-GB (S-CPGA-P13 X 13)

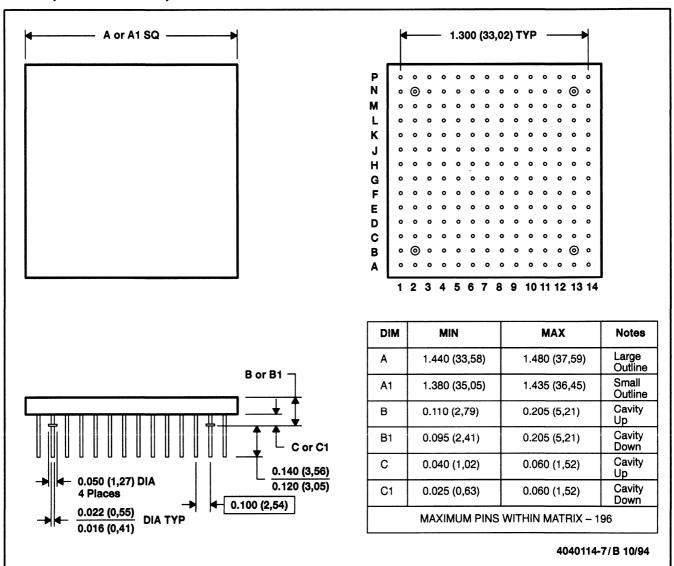
CERAMIC PIN GRID ARRAY PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark may appear on top or bottom depending on package vendor.
 - D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold plated or solder dipped.
 - G. Falls within MIL-STD-1835 CMGA5-PN and CMGA17-PN and JEDEC MO-067AE and MO-066AE, respectively

GA-GB (S-CPGA-P14 X 14)

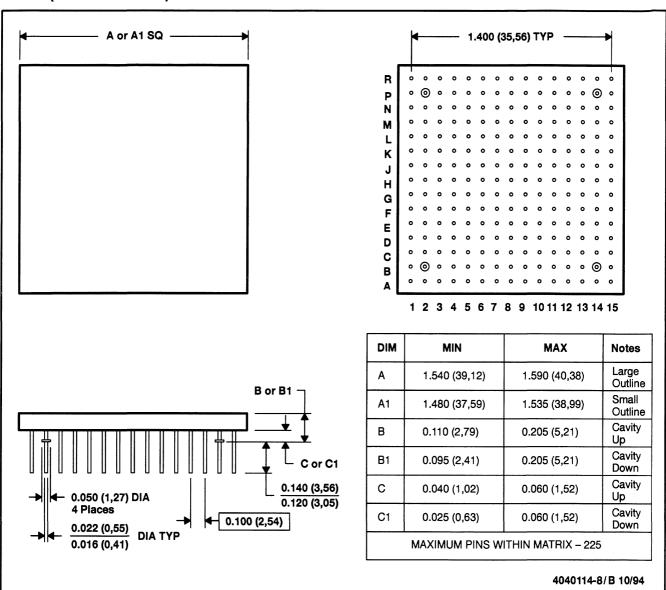
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA6-PN and CMGA18-PN and JEDEC MO-067AF and MO-066AF, respectively

GA-GB (S-CPGA-P15 X 15)

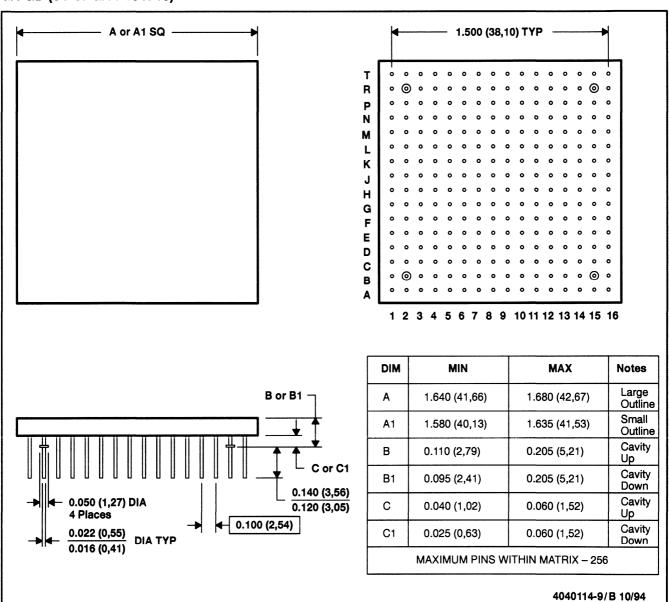
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA7-PN and CMGA19-PN and JEDEC MO-067AG and MO-066AG, respectively

GA-GB (S1-CPGA-P16 X 16)

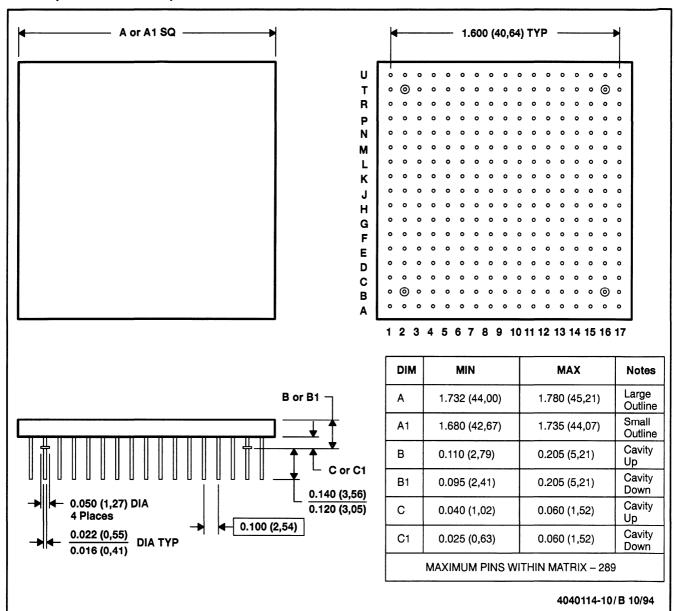
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA8-PN and CMGA20-PN and JEDEC MO-067AH and MO-066AH, respectively

GA-GB (S-CPGA-P17 X 17)

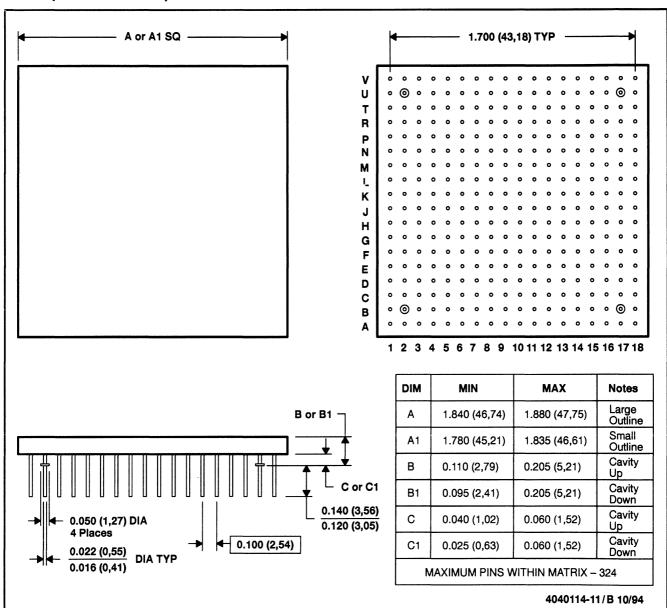
CERAMIC PIN GRID ARRAY PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark may appear on top or bottom depending on package vendor.
 - D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold plated or solder dipped.
 - G. Falls within MIL-STD-1835 CMGA9-PN and CMGA21-PN and JEDEC MO-067AJ and MO-066AJ, respectively

GA-GB (S-CPGA-P18 X 18)

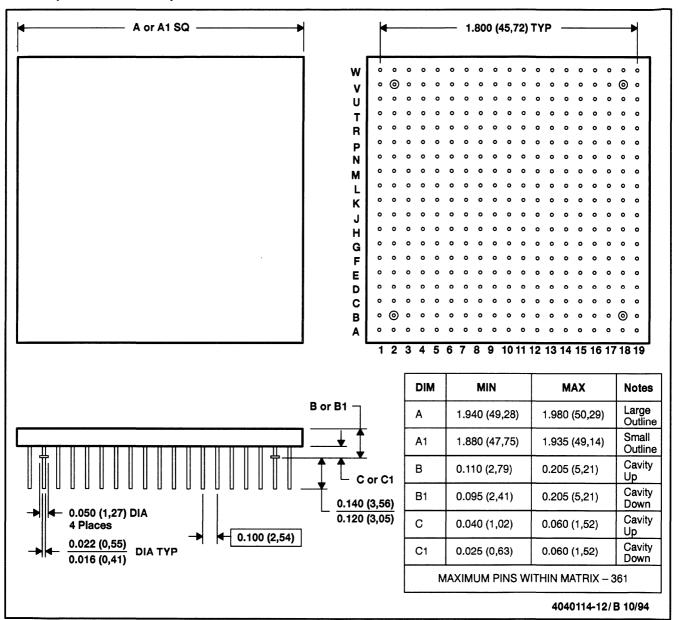
CERAMIC PIN GRID ARRAY PACKAGE



- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA10-PN and CMGA22-PN and JEDEC MO-067AK and MO-066AK, respectively

GA-GB (S-CPGA-P19 X 19)

CERAMIC PIN GRID ARRAY PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark may appear on top or bottom depending on package vendor.
 - D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold plated or solder dipped.
 - G. Falls within MIL-STD-1835 CMGA11-PN and CMGA23-PN and JEDEC MO-067AL and MO-066AL, respectively

CERAMIC PIN GRID ARRAY PACKAGE GA-GB (S-CPGA-P20 X 20) A or A1 SQ 1.900 (48,26) TYP W Ε D C В 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 DIM MIN MAX Notes B or B1 Large 2.080 (52,82) Α 2.040 (51,82) Outline Small **A1** 1.980 (50,29) 2.035 (51,69) Outline Cavity 0.110 (2,79) 0.205 (5,21) В Up Cavity 0.205 (5,21) **B**1 0.095 (2,41) 0.050 (1,27) DIA Down 0.140 (3,56) 4 Places 0.120 (3,05) Cavity С 0.040 (1,02) 0.060 (1,52) Up 0.022 (0,55) **DIA TYP** 0.100 (2,54) Cavity 0.016 (0,41) C1 0.025 (0,63) 0.060 (1,52) Down

NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Index mark may appear on top or bottom depending on package vendor.
- D. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
- E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
- F. The pins can be gold plated or solder dipped.
- G. Falls within MIL-STD-1835 CMGA12-PN and CMGA24-PN and JEDEC MO-067AM and MO-066AM, respectively

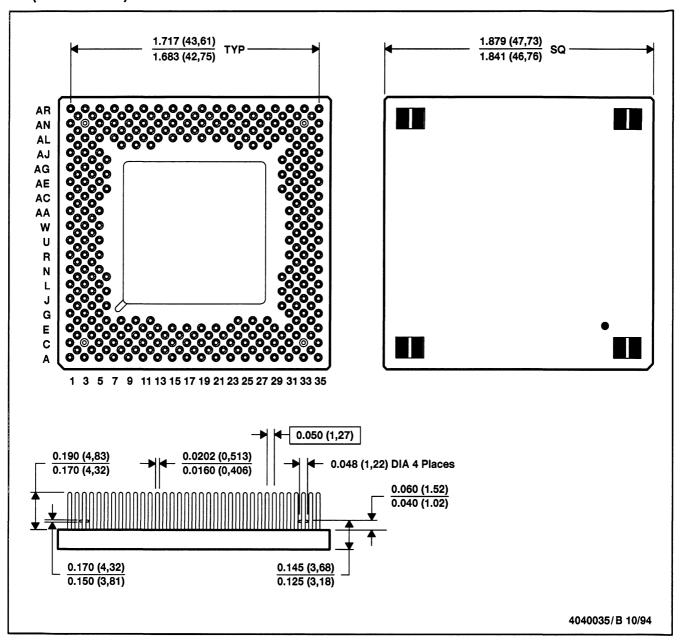


MAXIMUM PINS WITHIN MATRIX - 400

4040114-13/B 10/94

GF (S-CPGA-P325)

CERAMIC PIN GRID ARRAY PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

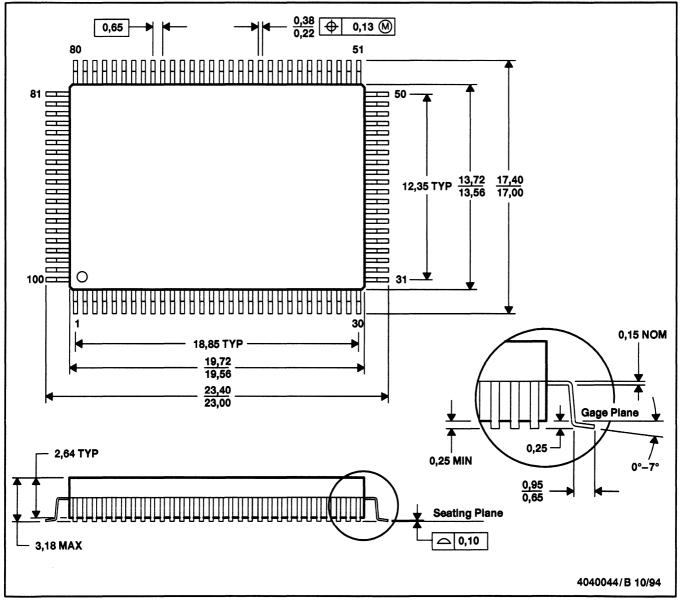
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	104		PA	4040036	6–24
	408		HDI	4040297	6–25
CSIP	30		AD	4040192	6-26
(CERAMIC SINGLE-IN-LINE PKG)	30		BD	4040196	6–27
	30		U	4040193	6–28
	72		ВК	4040197	6-29
	72		вк	4040226	6–30

MBM (R-MQFP-G100)

METAL QUAD (MQUAD®) FLATPACK (DIE-DOWN)



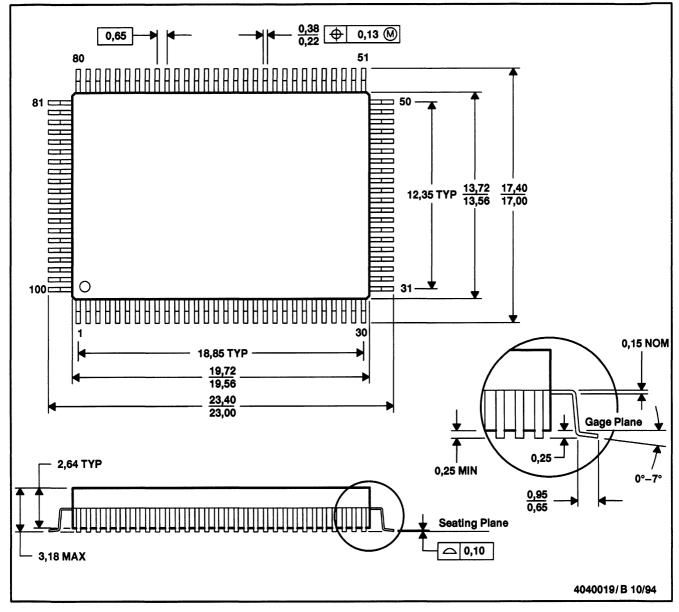
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



MBN (R-MQFP-G100)

METAL QUAD (MQUAD®) FLATPACK



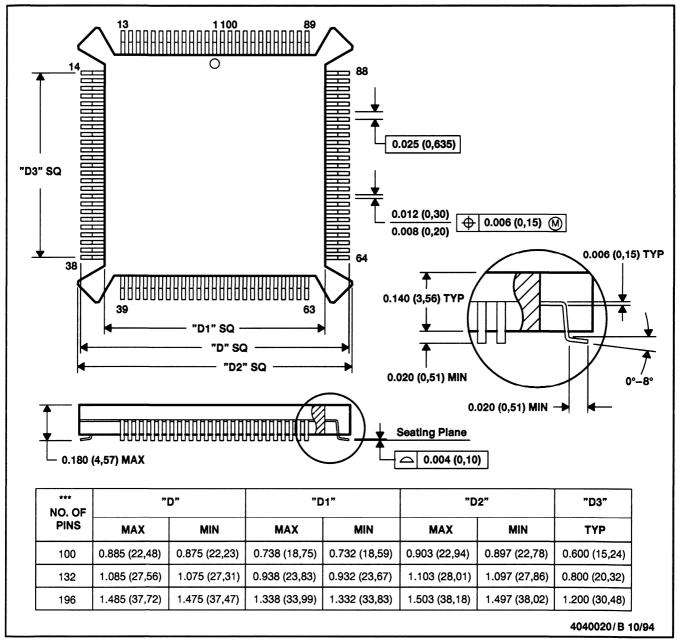
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by

MAA (S-MQFP-G***)

METAL QUAD (MQUAD®) FLATPACK (DIE-DOWN)

100 PIN SHOWN



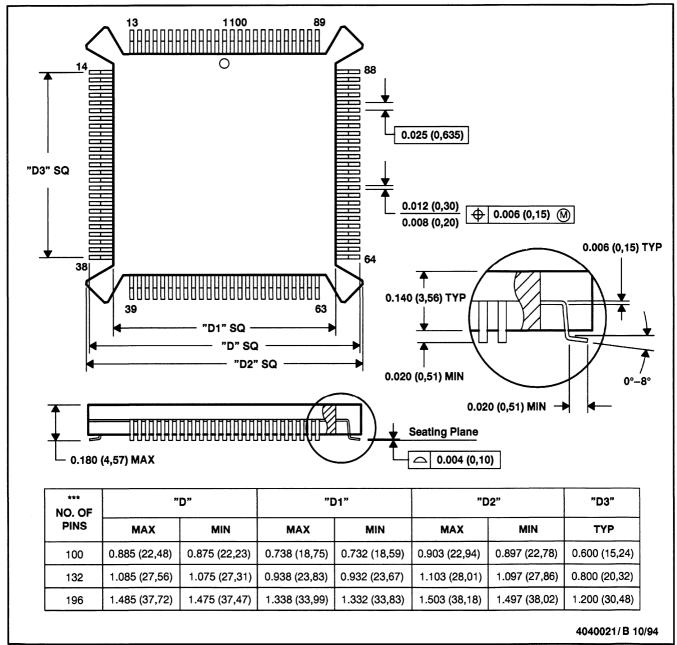
- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MQUAD is a registered trademark of Olin Corporation.
 - D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by



MAB (S-MQFP-G***)

METAL QUAD (MQUAD®) FLATPACK

100 PIN SHOWN

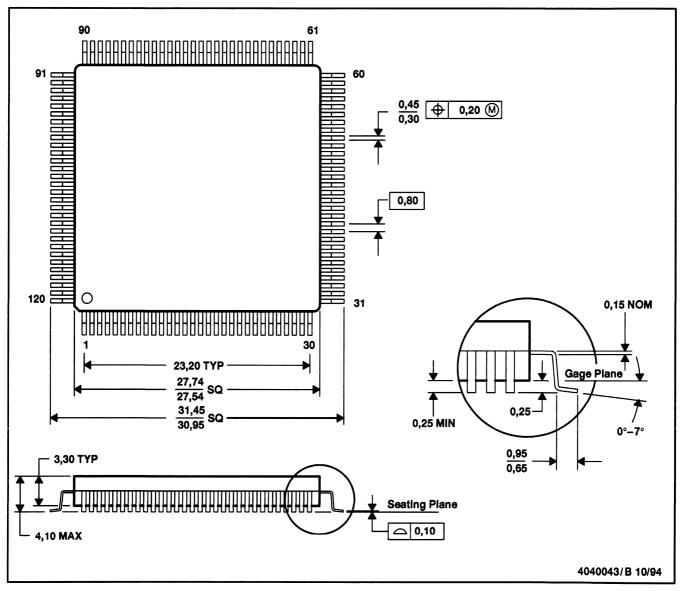


- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MQUAD is a registered trademark of Olin Corporation.
 - D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



MCM (S-MQFP-G120)

METAL QUAD (MQUAD®) FLATPACK (DIE-DOWN)

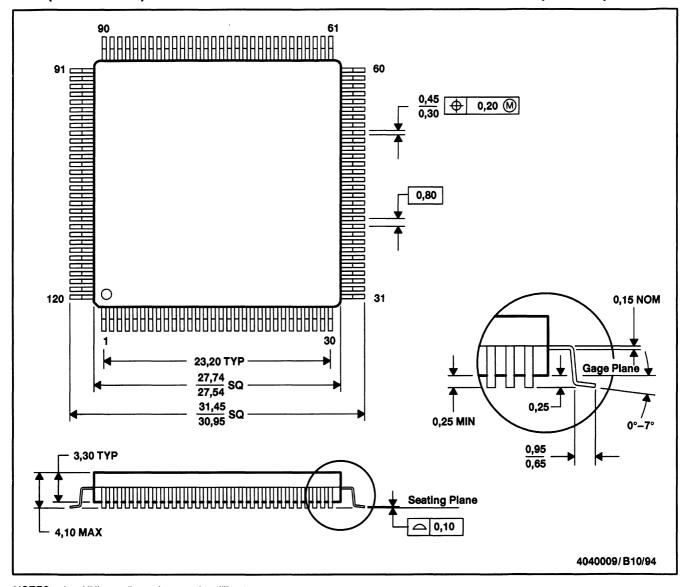


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.

MCN (S-MQFP-G120)

METAL QUAD (MQUAD®) FLATPACK



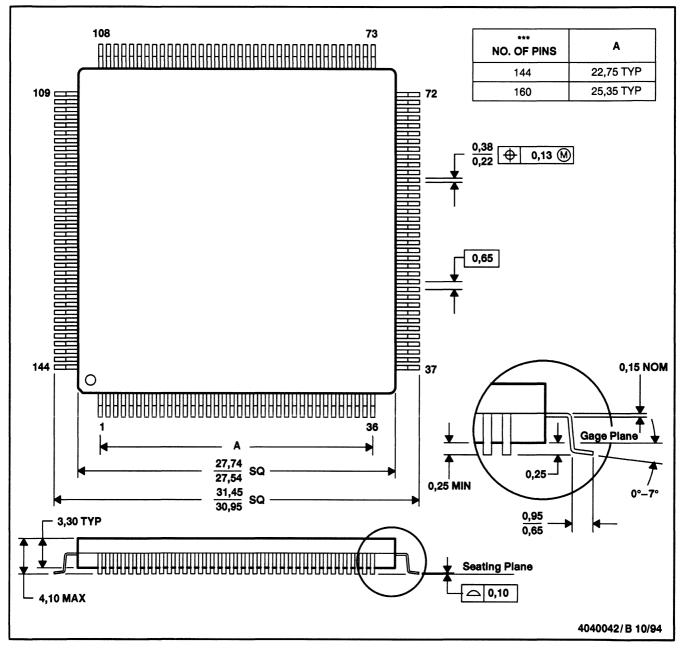
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.

MDM (S-MQFP-G***)

METAL QUAD (MQUAD®) FLATPACK

144 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

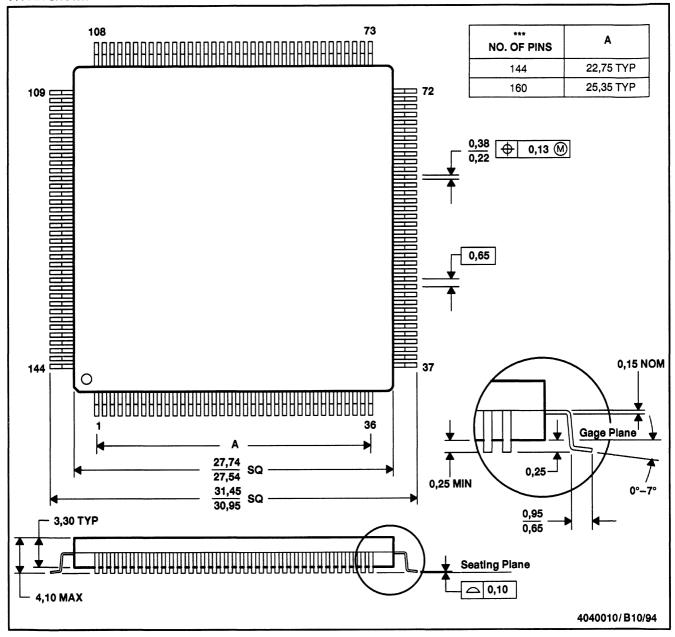
- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.
- E. The 144 MDM is identical to the 160 MDM except four leads per corner are removed.



MDN (S-MQFP-G***)

METAL QUAD (MQUAD®) FLATPACK

144 PIN SHOWN



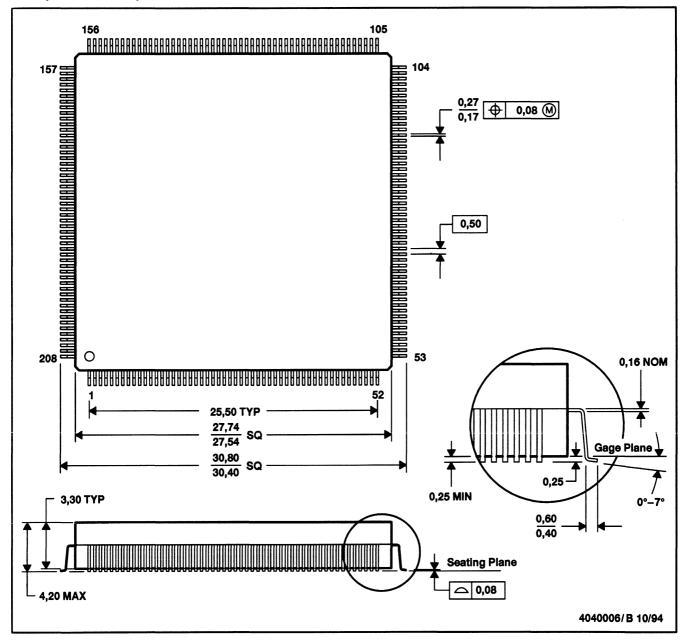
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.
- E. The 144 MDN is identical to the 160 MDN except four leads per corner are removed.



MEO (S-MQFP-G208)

METAL QUAD (MQUAD®) FLATPACK (DIE-DOWN)



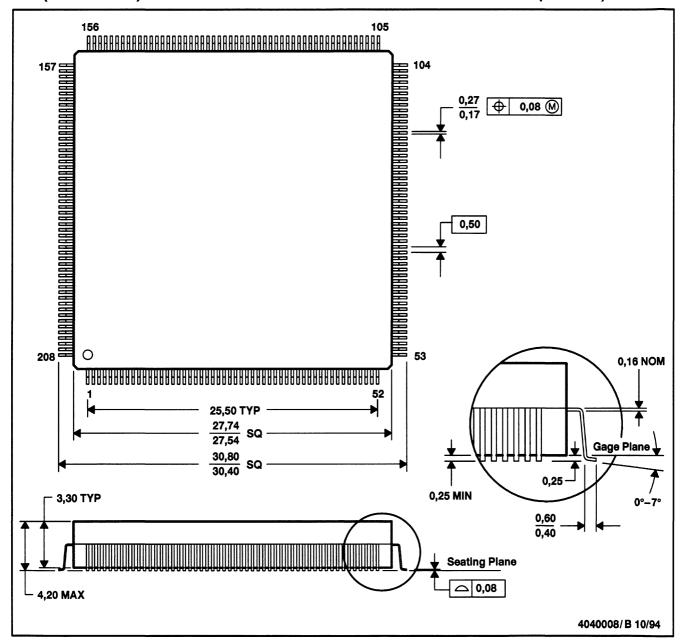
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



MEP (S-MQFP-G208)

METAL QUAD (MQUAD®) FLATPACK



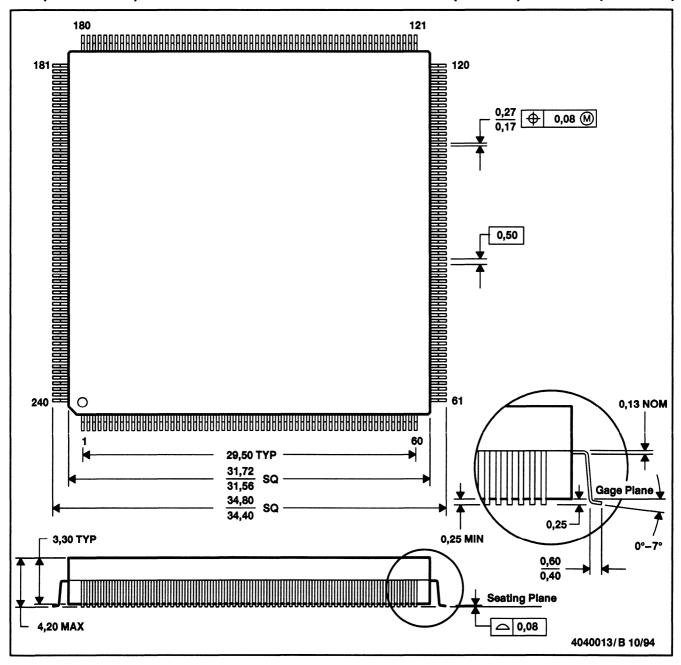
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



MFO (S-MQFP-G240)

METAL QUAD (MQUAD®) FLATPACK (DIE-DOWN)



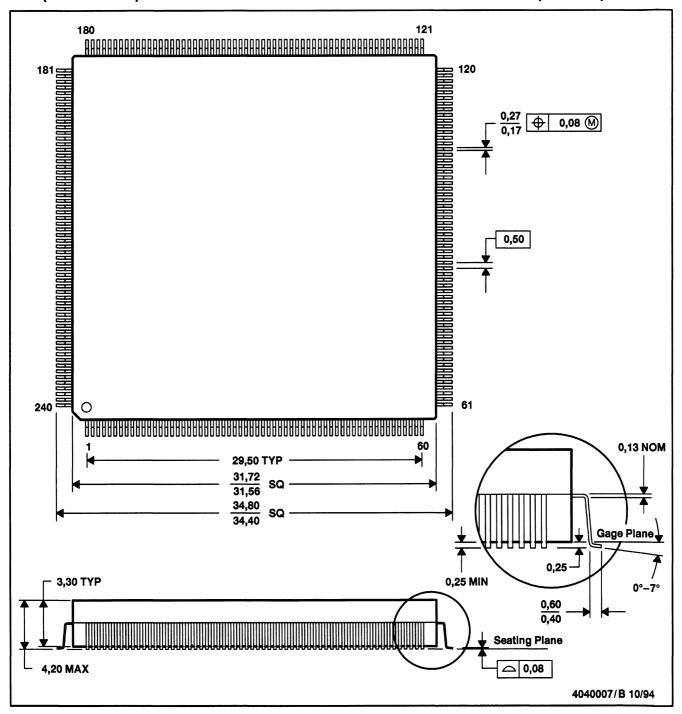
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



MFP (S-MQFP-G240)

METAL QUAD (MQUAD®) FLATPACK



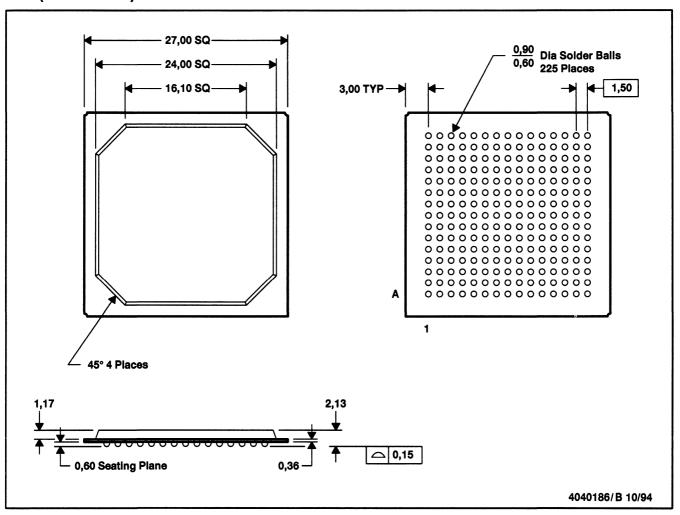
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. MQUAD is a registered trademark of Olin Corporation.
- D. This quad flatpack consists of a circuit mounted on a leadframe and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic.



GFM (S-PBGA-N225)

PLASTIC BALL GRID ARRAY

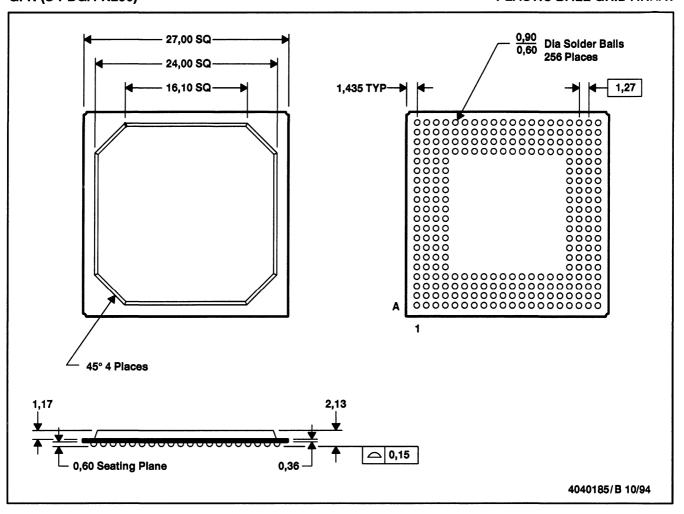


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

GFN (S-PBGA-N256)

PLASTIC BALL GRID ARRAY

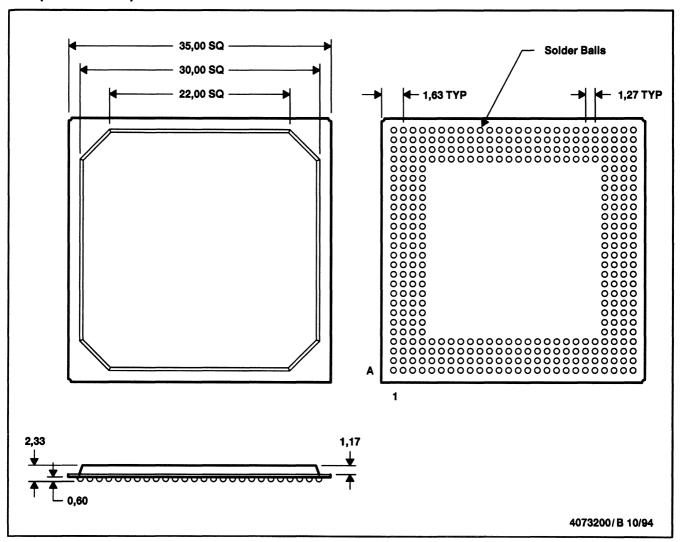


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

GFT (S-PBGA-N352)

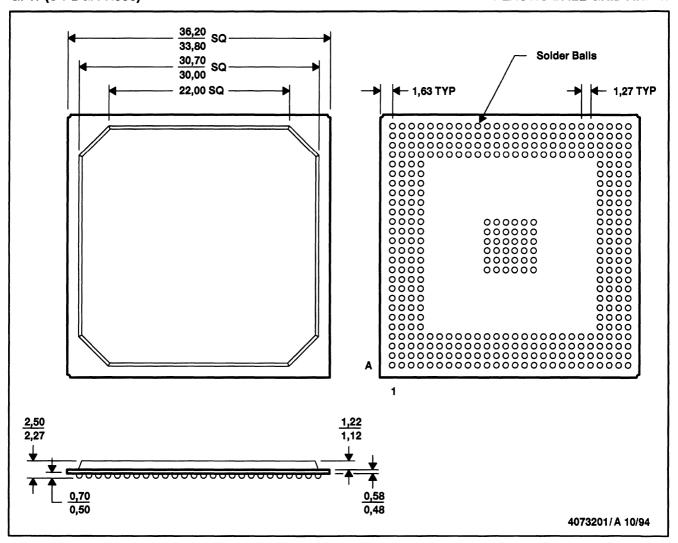
PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

GFW (S-PBGA-N388)

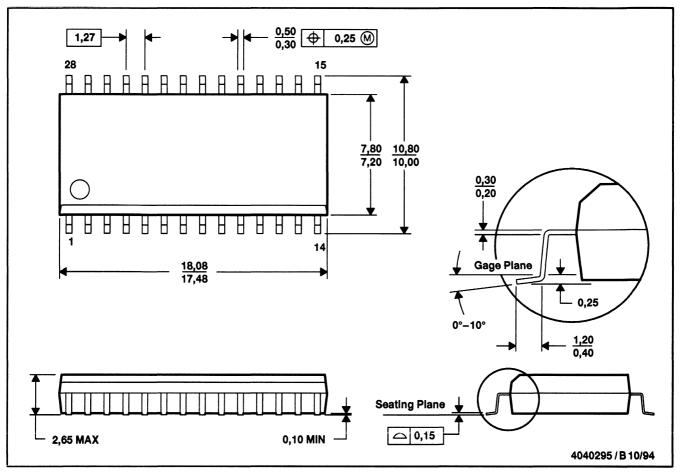
PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

DWM (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



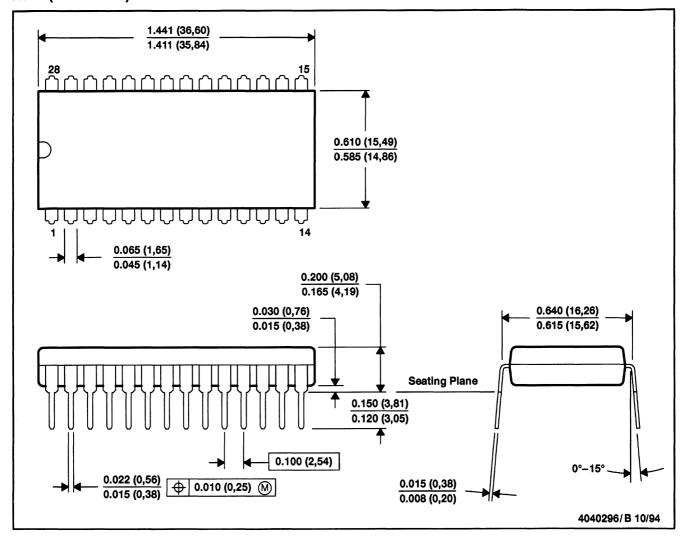
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions include mold flash or protrusion.

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NWM (R-PDIP-T28)

PLASTIC DUAL-IN-LINE PACKAGE

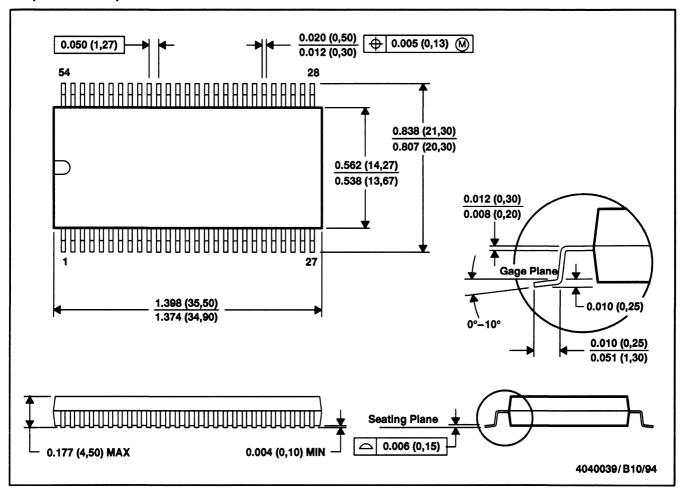


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.

PD (R-PDSO-G54)

PLASTIC DUAL SMALL-OUTLINE PACKAGE

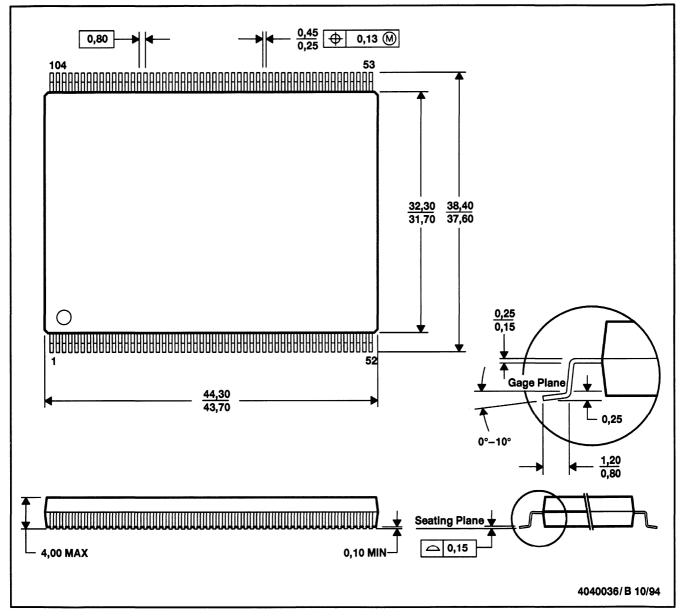


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is designed for a ceramic MCM substrate to be mounted on the lead frame pad and wire bonded to the lead fingers.

PA (R-PDSO-G104)

PLASTIC DUAL SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. This package is designed for a ceramic MCM substrate to be mounted on the lead frame pad and wire bonded to the lead fingers.

OCTOBER 1994

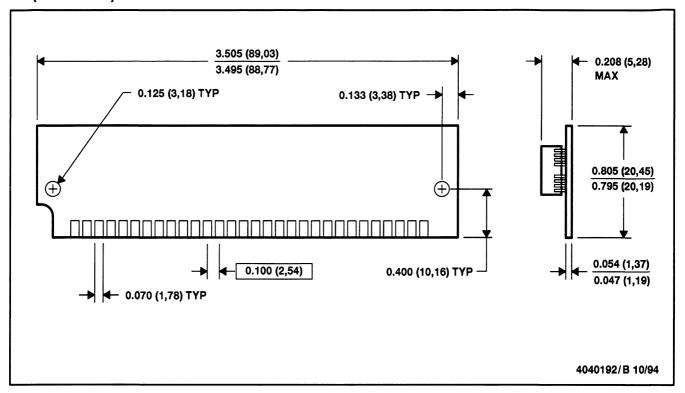
HDI (S-CQCC-N408) **CERAMIC MULTICHIP MODULE** - 0,254 1,270 - 0,432 50,800 102 1,270 4040297/B 10/94

NOTES: A. All linear dimensions are in millimeters.

OCTOBER 1994

AD (R-CSIP-N30)

SINGLE-IN-LINE MEMORY MODULE



NOTES: A. All linear dimensions are in inches (millimeters).

4040196/B 10/94

OCTOBER 1994

3.505 (89,03) 3.495 (88,77) 0.125 (3,18) TYP 0.133 (3,38) TYP 0.100 (2,54) 0.400 (10,16) TYP 0.208 (5,28) MAX

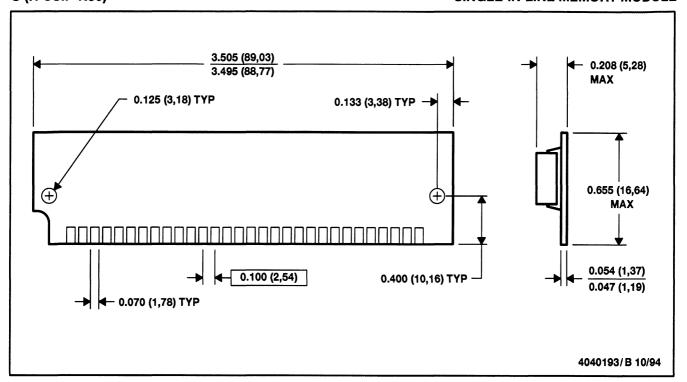
NOTES: A. All linear dimensions are in inches (millimeters).

← 0.070 (1,78) TYP

OCTOBER 1994

U (R-CSIP-N30)

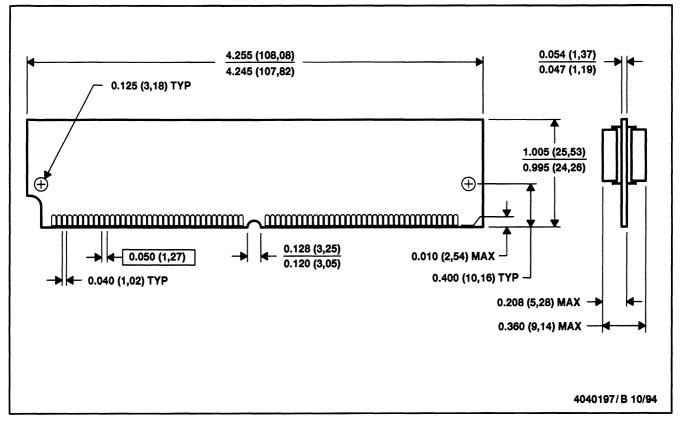
SINGLE-IN-LINE MEMORY MODULE



NOTES: A. All linear dimensions are in inches (millimeters).

BK (R-CSIP-N72)

DOUBLE-SIDED SINGLE-IN-LINE MEMORY MODULE

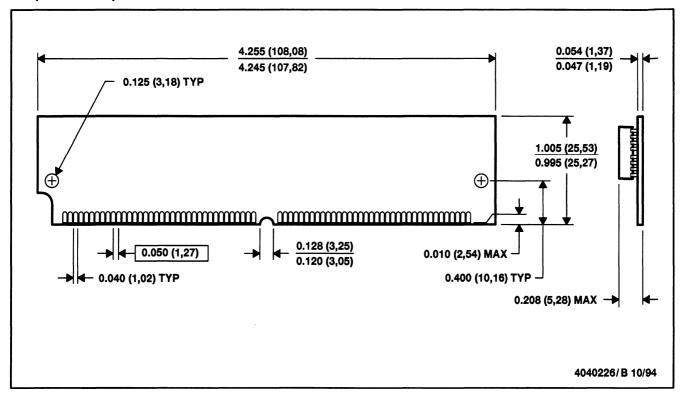


NOTES: A. All linear dimensions are in inches (millimeters).

OCTOBER 1994

BK (R-CSIP-N72)

SINGLE-IN-LINE MEMORY MODULE



NOTES: A. All linear dimensions are in inches (millimeters).

Appendix	7
Other Packages	6
Ceramic Through-Hole	5
Ceramic Surface-Mount	4
Plastic Through-Hole	3
Plastic Surface-Mount	2
General Information	1

Surface Mount Using Preplated Leadframes

To extend the life of surface-mount technology, the semiconductor industry is looking for methods to use lead-free solders and minimize the usage of chemicals, to reduce the outer pitch of surface-mount components without generating solder reflow problems, and to reduce cost, all without causing changes for customers. After several years of manufacturing experience, it can be stated that copper leadframes with palladium preplating fulfill these requirements and expectations.

Instead of conventional silver spot plating and post assembly solder plating, copper base metal leadframes can be flood plated with nickel and palladium to make a finish that is both wire bondable and solderable. A comparison between palladium finish and standard silver spot finish is schematically shown in Figure 1.

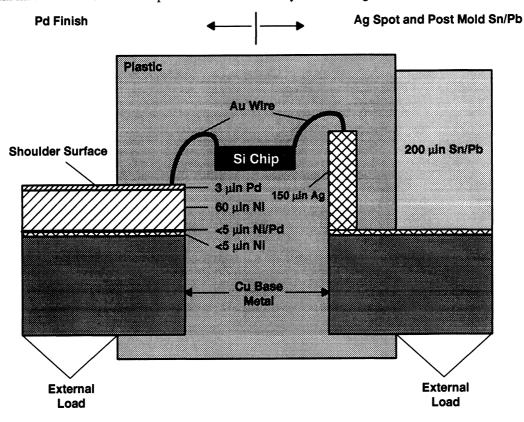


Figure 1. Palladium Versus Silver Spot Finish

With close to six billion palladium-finished devices in the field, the favorable experience can be summarized as follows:

- Eliminates Sn/Pb plating after molding
- No wet chemical exposure or thermal shock to finished device
- No Ag to Sn/Pb spot tolerance stack-up in preplated frames
- No solder flakes/burrs at trim/form
- Reduced mechanical damage
- Conformal coating minimizes handling transport jams
- Very thin coating with less absolute variability than Sn/Pb plate gives better lead tip planarity
- No cost for disposal of lead contaminated scrap
- No lead in manufacturing process and product
- No requirements for space, personnel, equipment, waste treatment, process water, utilities, or exhaust for Sn/Pb plating
- No environment permitting for solder plate process
- No QC for secondary process
- Reduces manufacturing cycle time
- Trim scrap value: roughly \$4 of Pd for every \$1 of Cu scrap. This must be netted against leadframe cost as well as cost for disposal of PB contaminated scrap.
- Excellent solderability of finished package
- Excellent adhesion for most molding compounds
- No dendritic Ag growth
- Compatible with existing assembly process, mount cure and mold, and with higher temperature bonding process, not limited by Sn/Pb eutectic
- Superior board mount results-strength and uniformity
- Particularly applicable to fine pitch packages. Very uniform solder joints. The only solder brought to the joint is that which is screened onto the board. Works well with lead-free solders.

ELECTROSTATIC DISCHARGE (ESD)

Introduction

In recent years, the semiconductor industry has made great strides in developing faster, lower power, and smaller devices. During the '90s, many devices will be produced with minimum feature size of structures on the silicon chip of 0.25 micron. To put this in perspective, a typical human hair is about 75 microns in diameter. However, as feature sizes get smaller and smaller, ESD sensitivity (voltage level at which the device will sustain damage) also gets lower. This means that ESD protection and ESD handling procedures will become even more important in the future to avoid ESD damage.

All semiconductor devices have an ESD voltage threshold above which they will sustain damage. While circuit designers can provide some on-circuit ESD protection (typically in the 2,000–4,000 volt range for the human body model and 200–300 volts for the machine model), this is well below the static voltage levels found in work areas without ESD protection. Proper ESD handling and packaging procedures must be utilized throughout the processing, handling, and storing of unmounted ICs and ICs mounted on circuit boards.



What is ESD and how does it occur?

Static charge is an unbalanced electrical charge at rest. It is created by insulator surfaces rubbing together or pulling apart. One surface gains electrons while the other surface loses electrons. This results in an unbalanced electrical condition recognized as static charge.

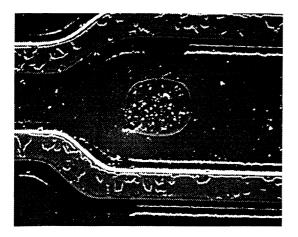
When static charge moves from one surface to another, it becomes ESD. ESD is a miniature lightning bolt of static charge that moves between two surfaces that have different potentials. It can only occur when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When static charge moves, it becomes a current that damages or destroys oxides, metallizations, and junctions. ESD can occur in any one of four different ways: a charged body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric sufficient to break it down.

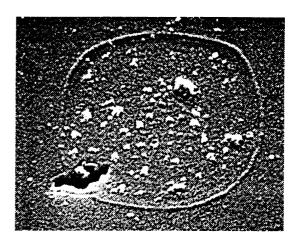
Latent Defects

Devices with latent ESD defects are called "walking wounded" because they have been degraded but not destroyed by ESD. This occurs when an ESD pulse is not sufficiently strong to destroy a device but nevertheless causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device still functions and is still within data sheet limits. A device may be subjected to numerous weak ESD pulses, with each one further degrading a device before it finally becomes a catastrophic failure. There is no known practical screen for walking wounded devices. In order to avoid this type of damage, devices must be continually accorded ESD protection as outlined later.

What voltage levels of ESD are possible?

It has been shown that human beings can be charged up to 38,000 volts just by walking across a rug on a low-humidity day. In order for an ESD pulse to be seen, felt, or heard, it must be in the range of 3000–4000 volts. Many devices can be damaged well below this threshold. ESD damage is shown in the failure analysis pictures on the next page.





Punctured Barrier Junction After ESD Test at 4000 Volts.

How to avoid ESD damage to ICs

Since ESD can occur only when different potentials are involved, the best way to avoid ESD damage is to keep the ICs at the same potential as their surroundings. The logical reference potential is ESD ground. So the first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them maintained at ESD ground potential. There are four supplementary rules that support this first rule.

- Any person handling the ICs should be grounded either with a wrist strap or ESD protective footwear used in conjunction with a conductive or static-dissipative floor or floor mat.
- The work surface where devices are placed for handling, processing, testing, etc., must, be made of static dissipative material and be grounded to ESD ground.
- All insulator materials must either be removed from the work area or they must be neutralized with an ionizer. Static generating clothing may be covered up with an ESD protective smock.
- When ICs are being stored, transferred between operations or workstations, or shipped, they must be maintained in a Faraday shield container whose inside surface (touching the ICs) is static dissipative.

Humidity

Where insulators are present, humidity is a very important factor in the generation of static electricity. Humidity affects the surface resistivity of insulator materials. As humidity increases, the surface resistivity decreases. This means that insulator materials rubbed together or pulled apart in a humid environment generate lower static charges than the same materials rubbed together or pulled apart in a dry environment. Where it is possible to control humidity, it is recommended that relative humidity be maintained between 40 percent and 60 percent. Higher humidity becomes very uncomfortable for humans, and lower humidity increases the risk of static generation from insulators. Humidity is a supplementary control and is not sufficient by itself to reduce static voltages to safe levels.

Training

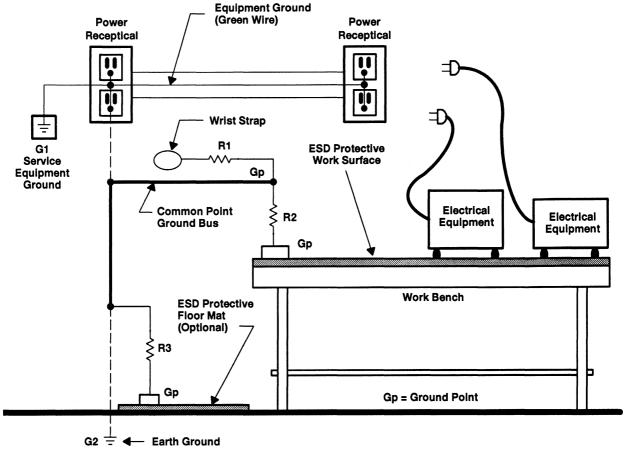
All personnel who come in close proximity with ESD-sensitive ICs must receive ESD training initially and then again each year as a minimum. No ESD program can be successful unless the people who handle the ICs understand the need for ESD controls.

ESD Specification

Each area handling ESD-sensitive devices is operated in accordance with the established ESD Handling Procedure. THe latest version of this controlled document is maintained in each area and is accessible to all area personnel.

ESD Coordinator

One person is identified who has overall responsibility for the ESD program. This person is responsible for writing the ESD Handling Procedure, keeping it updated, ESD training, and material evaluation.



NOTES: 5. G1 (equipment ground) or G2 (earth ground) is acceptable for ESD ground. Where both grounds are used, they shall be connected (bonded) together.

- 6. R1 is mandatory for all wrist straps.
- 7. R2 (for static dissipative work surfaces) and R3 (for ESD protective floor mats) are optional. ESD protective flooring shall be connected directly to the ESD ground without R3.
- 8. This ESD-protected workstation complies with JEDEC Standard No. 42.

Figure 6. ESD-Protected Workstation (Side View)

Audits

Periodic audits ranging from daily to yearly are held to ensure that all ESD handling procedures are being followed and that all ESD materials (wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD Handling Procedure

The TI worldwide ESD Handling Procedure is available to customers upon request.

Moisture Sensitivity of Plastic Surface-Mount Packages

Some plastic surface-mount packages are classified as moisture sensitive because the moisture that has been absorbed inside the package can expand rapidly during exposure to the high temperature stress of reflow soldering and create mechanical damage to the package (often referred to as popcorn). Surface-mount packages are subjected to much higher solder reflow temperatures than their through-hole counterparts. The bodies of the through-hole parts are shielded from the hot wave solder by the PC board, while surface-mount parts have their bodies subjected to the solder reflow temperature.

All plastic packages absorb some moisture at room ambient conditions. The amount of moisture that is absorbed is based on a number of factors including the room temperature and humidity. However, there is no threshold level of moisture absorption or gain that applies to all plastic surface-mount packages and makes them moisture sensitive. Conversely, all plastic surface-mount packages that are essentially moisture free at the time of reflow solder will be free of moisture-induced stress failures.

It is important, therefore, to know which packages are tested for moisture sensitivity so they can receive special care in handling to minimize moisture absorption and subsequent moisture-induced stress damage during the reflow solder operation.

At Texas Instruments, plastic surface-mount packages are tested for moisture sensitivity using JEDEC Test Method A112, Moisture-Induced Stress Sensitivity for Plastic Surface-Mount Devices. Packages that are found to be moisture sensitive are baked (to drive out the moisture) and then placed in a protective dry-pack bag that contains a humidity indicator card and sufficient desiccant to maintain a very low humidity level in the bag. A caution label (as defined in JEDEC Publication No. 113) is attached to the bag and indicates the minimum floor life of the packages once they are removed from the protective dry environment of the bag.

Plastic surface-mount packages that are not moisture sensitive per JEDEC Test Method A112 do not need to be dry packed or handled in a special way to minimize moisture absorption prior to reflow soldering provided that the package body temperature does not exceed 220°C (this is the JEDEC Test Method A112 evaluation temperature).

Test Structures

Test structures for packaging applications are designed to either measure a particular quantity directly or to detect a failure mechanism. Strain gauges that give quantitative values of either compressive or tensile stresses are an example of the first type of structure. Moisture sensors that measure the amount of harmful ionic contaminates within a package by resistively monitoring aluminum corrosion are an example of the second type of test structure[1], [2], [3].

Characteristics of a well designed package test structure are: 1) the structure should be sensitive only to the effect to be measured, 2) the structure should give repeatable quantitative results, and 3) the structure should be positioned on the chip for maximum sensitivity. The first goal can be achieved by designing the structure to be more sensitive to the measured quantity than to anything else. For example, a strain gauge should have a high enough resistance to minimize experimental errors that might result from contact resistances or resolution limitations of the test instrument. The second goal is sometimes more elusive but can usually be achieved by simplification of the structure or by the inclusion of on-chip buffer circuitry to isolate the structure from the vagaries of test fixtures. For example, corrosion due to contamination can be monitored by measuring the continuity of a narrow, long metal line without on-chip circuity. On the other hand, to monitor the impact of packaging on device speed, buffers would be required to isolate the on-chip oscillator from capacitance loading by the test fixture.

Results are obtained through experimentation. The structures are packaged in the materials and designs of interest. Comparisons are made between results with the new materials or designs and control groups using known materials or designs. Acceleration of failure mechanisms is usually required to assess the reliability of the new assemblies. Selection is then made of the best materials and designs, resulting in a package ready for qualification.

Stress Sensitive Test Structures Used by Industry

Diffused Strain Gauges. Diffused strain gauges have been widely used for the past seven or eight years to measure package stresses [3]–[7]. Each diffused strain gauge measures the stress averaged across the gauge at its position on the chip. Small gauges locate the stress quantity more precisely than do large gauges. A mapping of stress on the chip can be made by placing a number of gauges at different locations; for example, in the corner of the chip, along the edges, and at the center. Designers should ensure that interconnect resistance is orders of magnitudes less than the resistance of the gauge itself.

The diffused strain gauge detailed in Figure 1 is typical. It is formed by an implanted N-type resistor on (100) silicon. Since crystalline silicon is a piezoresistive material, the mobility of charge carriers, and hence the resistance of the diffusion, is modulated by the mechanical stress applied to the crystal lattice. The amplitude and sign of the resistance modulation is a function of the following factors: dopant type and concentration profile, the crystalline orientation of the silicon, and the nature of the stress, either compressive or tensile. For N-type diffusions or implants, positive resistance changes are indicative of compressive stress applied to the chip during the assembly operation. Negative resistance changes indicate tensile stress. The resistance shifts for this gauge are related to the stress in the various crystalline axes by the following equations [11].

$$\frac{\Delta R}{R_{01'}} = \pi_{11'}\sigma_{1'} + \pi_{12'}\sigma_{2'} + \pi_{13'}\sigma_{3'}$$

$$\frac{\Delta R}{R_{02'}} = \pi_{21'}\sigma_{1'} + \pi_{22'}\sigma_{2'} + \pi_{23'}\sigma_{3'}$$
[8]

Where:

 π_{11} , = piezoresistance coefficient

 σ_{1} , = compressive (negative) or tensile (positive) stress

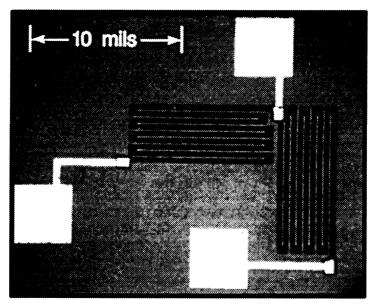


Figure 1. Detail of Diffused Strain Gauge

Note that there are three unknown stresses and only two equations. A third equation would represent the resistance shift in the direction perpendicular to the chip surface. Since it is impossible to measure this shift with planar processing, finite element analysis (FEA) calculated average value of perpendicular stress is chosen so that the remaining stresses may be estimated. Typically, this normal stress is an order of magnitude less than the planar stress at any point on the chip except at the edges (see Figure 2). This assumption leads to error in the quantitative stress measured by the strain gauge.

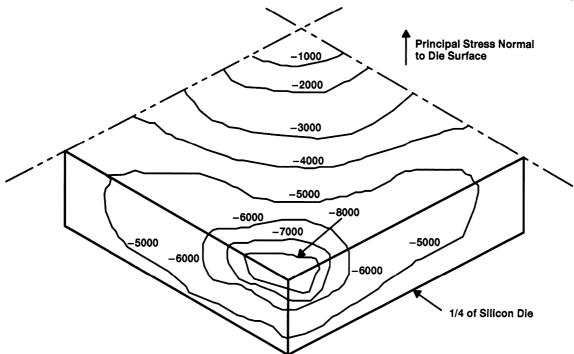


Figure 2. Contours for Compressive Stress Normal to Chip Surface

Note also that no torque or shear stresses show up in the equations above. These terms are a function of the crystalline orientations and dopant types chosen for the strain gauges. For this particular gauge in (100) silicon, these terms were zero. Others have used gauges in different orientations, giving different sensitivities [7], [12]. One unique strain gauge uses both N- and P-type diffusions, which allows calculation of both the shear stress and the normal stress [9]. There is a trade-off, however, in that more complex gauges require more leads, limiting the number of gauges that can be arrayed on the chip and bonded at one time. Much interesting information can be found by examining the mapping of stress as found through a strain gauge array (see Figure 3).

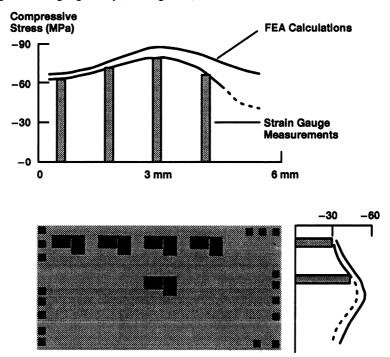
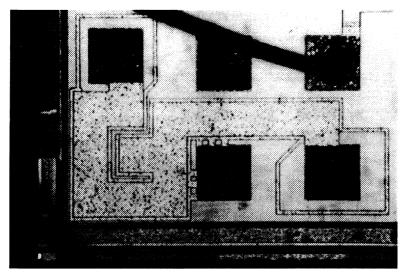


Figure 3. Mapping of Stress Using Strain Gauges Arrayed on Chip. Comparison Made to FEA Results.

Experimental details to bear in mind when using diffused strain gauges include correcting for temperature shifts. This can be done by using on-chip bridge arrangements or by measuring the chip temperature at test and correcting the data based on known temperature sensitivity.

Shear Stress Sensitive Test Structures. The shear stress structures discussed here are typical of those used throughout the industry [10], [11]. Since shear stress affects the passivation over wide metal and the circuitry beneath, a major feature of both structures is a wide metal line. Since the shear stress is greatest at the corner of the chip, both are designed in the corner. They detect the effects of shear stress rather than measuring the absolute magnitude of the shear stress. They provide both electrical and visual data on the shear stress effects.

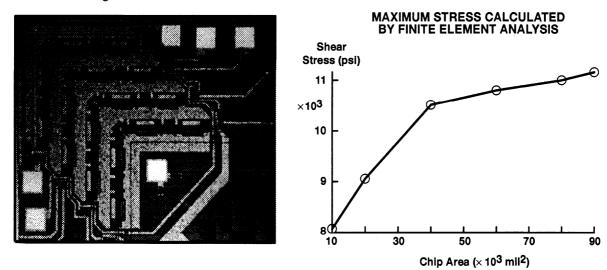
The first shear stress structure (see Figure 4) was designed to detect shorting between a wide metal line subject to shear stress damage and a narrow sense line. The wide line, designed to simulate a worst case power bus layout was 102 microns across. The 10-micron sense line was separated from the wide bus by a 3-micron space.



NOTE A: The 102-micron bus line surrounded by the 10-micron sense line. This was intended to be a worst case design and is intentionally close to the corner.

Figure 4. Wide Metal Visual Shear Structure in Corner of Chip

The second shear stress structure (see Figure 5) was designed to detect damage to polysilicon running under the edges of wide metal. The major unit of the structure was a 100-micron-wide metal line with an extensive poly snake running under it. The poly snake was 3.5 microns wide with 3.5 microns spacing. Electrical contact was made to both ends of the poly snake, allowing continuity measurements. This unit was then duplicated four times at multiples of 150 microns, which allowed a determination of the shear damage as a function of distance from the corner. The extra leads seen in the figure contact source and drain diffusions under the poly snakes and allowed measurement of transistor characteristics during test.



- Test structures measure shear stress in critical chip zones
- Stress data are compared for chips of various areas
- Stress failures minimized by design rules and material selection

Figure 5.

References

- [1] N. L. Sbar and R. P. Kozakiewicz, "New Acceleration Factors for Temperature, Humidity, Bias Testing", 16th Annual Proceedings, Reliability Physics 1978, IEEE Catalog No. 78CH1294-8, pp. 161–178.
- [2] R. G. Mancke, "A Moisture Protection Screening Test for Hybrid Circuit Encapsulants", *Proceedings of the 31st Electronic Components Conference*, Atlanta, GA, 1981, pp. 119–125.
- [3] D. Edwards, et al., "Test Structure Methodology of IC package Material Characterization", *Proceedings of the* 33rd Electronic Components Conference, 1983, pp. 386–393.
- [4] J. L. Spencer, et al., "New Quantitative Measurement of IC Stress Introduced by Plastic Packages", *Proceedings of the 19th Annual Reliability Physics Symposium*, 1981, pp. 74–80.
- [5] W. H. Schroen, et al., "Reliability Tests and Stress in Plastic Integrated Circuits", *Proceedings of the 19th Annual Reliability Physics Symposium*, 1981, pp. 81–87.
- [6] R. J. Usell and S. A. Smiley, "Experimental and Mathematical Determination of Mechanical Strains within Plastic IC Packages and Their Effect on Devices During Environmental Tests", *Proceedings of the 19th Annual Reliability Physics Symposium*, 1981, pp. 65–73.
- [7] B. Natarajan and B Bhattacharyya, "Die Surface Stresses in a Molded Plastic Package", *Proceedings of the 36th Electronic Components Conference*, 1986, pp. 544–551.
- [8] J. Spencer, "Calculating Stress and Mobility in Silicon Chips Using Strain Gauge Measurements", TI Semiconductor Engineering Journal, Vol. 1, 1981, pp. 34–37.
- [9] H. Miura, et al., "Development and Application of the Stress Sensing Test Chip for IC Plastic Packages", 64th Annual Meeting, Japan Society of Mechanical Engineers, (April 1987).
- [10] D. R. Edwards, et al., "Shear Stress Evaluation of Plastic Packages", Proceedings of the 37th Electronic Components Conference, 1987, pp. 84-95.
- [11] C. G. Shirley and R. C. Blish, II, "Thin-Film Cracking and Wire Ball Shear in Plastic DIPs Due to Temperature Cycle and Thermal Shock", *Proceedings of the 25th Annual Reliability Physics Symposium*, 1987, pp. 238–249.
- [12] C. G. M. van Kessel, S. A. Gee, and J. J. Murphy, "The Quality of Die-Attachment and it's Relationship to Stress and Vertical Die-Cracking", *Proceedings of the 33rd Electronic Components Conference*, 1983, pp. 237–244.

Glossary

Ball Grid Array (BGA)

Surface mountable package with solder balls as leads attached to the bottom of the package

Ceramic

Inorganic, nonmetallic material, such as alumina or beryllia

CERDIP

Dual-in-line package consisting of a leadframe encased with a ceramic shell

Coplanarity

Distance from the seating plane to the lead farthest from the seating plane

DIP

Dual-in-line package designed with leads for through-hole mounting. Lead pitch is 2.54 mm (0.100 inch)

Gage Plane

A plane established above the seating plane to be used as a standard for measuring lead length

Heat Sink

Heat conductive material used to transmit heat from the silicon chip to the external environment. Usually a heat sink is made of metal.

Heat Slug

Heat sink that is exposed to the external environment

Heat Spreader

Heat sink that is internal to the package

Heat Dissipating QFP (HQFP)

Quad flat pack designed with a heat sink

Heat Dissipating SOP (HSOP)

Small-outline package designed with a heat sink

Heat Dissipating SSOP (HSSOP)

Shrink small-outline package designed with a heat sink

Hermetic

Seal so that package is not penetrable by moisture vapor or other gases

JEDEC

Joint Electronic Device Engineering Council

J-Lead

Leads formed into a J pattern

Lead Frame

The metallic portion of the package that completes the electrical path from the internal package to the external

Leadless Ceramic Chip Carrier (LCCC)

Ceramic package having metalized contacts at its periphery instead of wire leads

Mold Flash

Thin layer of mold compound that extends from the sides of the package onto the leads and/or between the leads generated during encapsulation

MQUADTM

Quad flat pack style package with a metal shell as opposed to plastic

Multichip Model

A module or package capable of supporting several chips on a package

Nom

Abbreviation for nominal

Nominal

Average value for a given measurement

Pin Grid Array (PGA)

A package with pins extending from the bottom of the package

Plastic

A polymeric material used for encapsulation. Also known as mold compound

Plastic Flange Mount (PFM)

Through-hole package with a tab for thermal heat dissipation

Plastic Leaded Chip Carrier (PLCC)

Plastic package designed for surface mounting with J-lead configuration

Quad Flat Pack (QFP)

Package with leads extending from four sides in a gull lead form

Seating Plane

A plane generated, when the package is at rest, between the bottom of leads and the contact surface

Shrink Dual-In-Line Package (SDIP)

Package designed with leads for through-hole mounting. Lead pitch is 1.78 mm (0.70 inches).

Side Brazed

Technique where leads are attached to the ceramic package by brazing instead of being part of a lead frame

Single In-Line Package (SIP)

Package with leads only on a single side in one row

Small-Outline Package (SOP)

Plastic dual-in-line package with gull lead form that has a lead pitch less or equal to 0.65 mm (0.026 inches)

Solder Dip

Solder lead finish that is applied by dipping the leads into solder

Surface-Mount Package

Packages designed to mount onto, rather than into, the printed circuit board

MQUAD is a trademark of Olin Corporation, registered in the U.S.A.

Thin Quad Flat Pack (TQFP)

Quad flat pack with a total maximum height of 1.6 mm (0.63 inches)

Thin Shrink Small-Outline Package (TSSOP)

Plastic dual-in-line package with gull lead form that has a maximum height of 1.2 mm (0.048 inches) and a lead pitch less than or equal to 0.65 mm (0.026 inches)

Thin Small-Outline Package (TSOP)

Plastic dual-in-line package with gull lead form that has a maximum height of 1.2 mm (0.048 inches)

Through-Hole Package

Package designed to mount into the printed circuit board via plated holes in the board

Typ

Abbreviation for typical

Typical

Dimension or measurement is applicable for all other similar features

Zig-Zag In-Line Package (ZIP)

Package with leads from one side but the leads are formed into two rows, creating a zig-zag affect

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